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Power Optimization of Structural FIR Filters Using Data-Driven Clock Gating and Multi bit Flip-Flops

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Abstract: *Modern digital signal processing (DSP) architectures often prioritize power efficiency. Much study has focused on finding ways to optimize the power consumption of the digital finite duration impulse response (FIR) filter, which is a fundamental component of digital signal processing (DSP). Many people talk about and employ data-driven clock gating (DDCG) and multi bit flip-flops (MBFFs) as low-power design solutions. The FIR filter may be able to further reduce power use as it integrates numerous strategies into one algorithm. When testing the proposed FIR filter vs the conventional design, the results show a 25% and 22% reduction in power consumption, respectively.*

I. INTRODUCTION

Power consumption is an important consideration in the design of electrical devices such as mobile phones. In digital electronic circuits, power management might be static, dynamic, leaky, or short-circuit based on the scenario. Benefiting greatly from low static power consumption are complementary metal-oxide semiconductor (CMOS) very large scale integration (VLSI) circuits. The dynamic power use is caused by the maximum switching rate of the clock signal. Due to its guaranteed linear phase and stability, finite impulse response (FIR) filters are heavily used in digital signal processing (DSP) circuits. Audio processing, channel equalization, software defined radio (SDR), and high-efficiency video coding (HEVC) are some of the many modern mobile computing and portable multimedia applications that rely on these circuits. The same logic behind why scientists have been trying to find ways to lower the FIR filter's power usage applies here. The far-infrared (FIR) filters used in

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reconfigurable electronics have several uses, including the SDR channelize.

At the beginning, you have two options. The power consumption of the FIR filter was reduced by the authors of [3,4] by reducing the filter coefficients without affecting their order. As stated in [5], an approximation strategy is used in signal processing. The building of the filter is made somewhat easier by using add and shift operations. Numerous techniques are used in low-power design [6]. In the LNS sector, integer linear programming (ILP) was proposed in [7] to facilitate the quick creation of finite word length linear-phase FIR filters. In [8], there was some variation in the input word lengths and filter taps. In [9], we see a way to depict reduced dynamic signals. The authors of [10] employed a technique that could be turned backwards. A FIR filter using memristors is suggested in reference [11].Using an MBFF to increase FIR power was first described in [12].Power digital filters may be improved using the data-driven clock-gating (DDCG) technique [13].

Digital filters might benefit from clock gating, according to much research done in the last decade. Additional details about data-triggered clock gating digital filters may be found in [14].

In this study, we provide a hybrid method for reducing power consumption, which combines MBFFs and DDCG techniques to construct a highly efficient FIR filter.

A synopsis of the remaining sections of the work is included below. An introduction to the present FIR filter is given in Section 2.

II Back ground and Existing FIR Filters

An N-th-order FIR filter may apply filters coefficients to fresh input samples by applying N-point linear convolution on the input sequence. Linearly invariant Fourier transform infrared (FTIR) filters' transfer functions are:

$$y(x)\square \sum_{k=0}^{N-1} h_k x(n-k), \qquad (1)$$

Where x (n−k) are the input data at time instant (n − k), where N is the length of the filter and h is the k th coefficient.

This data's z-transform output is

$$y(z)\square H(z)X(z), \qquad (2)$$

Slower, power-hungrier, and with higher overhead are FPGAs compared to ASICs. Reworking the method won't make much of a difference because of its generalizability and reconfigurability.

The direct form (DF) and the transposed direct form (TDF) are two ways to build a

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filter. You can see this clearly in images 1 and 2.

Starting off with the FIR filter's DF structure and progressing to its TDF. Federal Information Reports (FIRs) in both its reversed and reversed versions

Figure 5 shows the filter's construction for an odd order N. Without the tap, Figure 5 displays a comparable structure.

Alike to filtering. Figure 1 show how the indirect form makes it easy to display the word length of each delay.

The number one is divided into four equal parts. How much does h2 equal? It is understood.

Occurred for a natural integer N of even order.

Its component has the same word length as the incoming signal. The word lengths of each delay element are obviously larger in the transposed version compared to the straight form. Additional features allow you to defer product or aggregation delays. Although the transposed architecture requires more circuitry, it reduces the critical route time. There is one multiplier and (M−1) adders in the DF along the key path, in contrast to the TDF's one multiplier and one adder. The performance gain is readily apparent for big M.

In comparison to the direct counterpart, the TDF performs better when it comes to VLSI implementation because of its incorporated pipelined accumulation component. Product accumulation and multiple constant multiplications are the two modules that make up a TDF's filter output. Over the last decade, the MCM module has seen a remarkable reduction in complexity.

III Power Optimization by Clock Gating Technique

Clock gating is one method for reducing power loss in clock signals.

It is clear that the output and input values are identical when two continuous inputs are utilized by comparing the present and future states of the D flip-flop. No matter how stable the inputs are from one clock to another, the latch will continue to deplete the power supply of the clock endlessly.

Primarily, the clock controller block is responsible for:

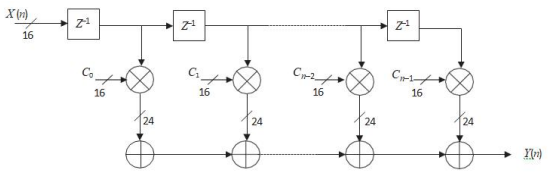

FIG1: Direct form low-pass FIR filter architecture.

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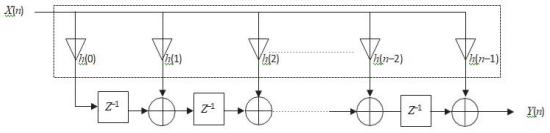

FIG2: Transposed direct form FIR filter architecture

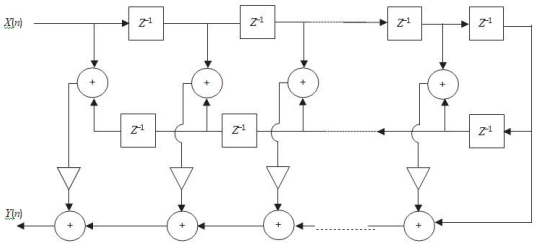

FIG3: The symmetric structure of the linear-phase FIR filter.

While the clock is running at period Tn, it checks whether the data input from the FIR block is the same as the data input from periods Tn−1 that came before.

Section two Once the clock controller confirms (i), it cuts power to the FIR filter.

There are essentially three types of clock gating approaches:

Techniques based on the combination of several components: The clock allows the signals to be synthesized in line with the logic of the underlying system.

IV Power Optimization by MBFF Technique

Rhythms that match the fiction-time. The objectives of MBFFs were making greater use of routing resources, optimizing clock latency, and controlling clock skew. The MBFF works in RTL.

Thus that it takes some time for Q to send the watch to U. For any given rising or falling time, the driving capabilities of a clock buffer are defined as the number of minimum-sized inverters it can drive. To get around this issue and conserve electricity, you may share a clock buffer with many flip-flops. The internal layout of the 1-bit and 2-bit flip-flops may be seen in Figure 6. If you want to lower the overall power consumption, you may swap out the two 1-bit flip-flops in Figure 6(a) with a 2-bit one. Two 1-bit flip-flops share a single clock buffer, which is why this is implemented.

The optimal FF design for lowering power consumption is detailed in [19].

V Implementation Methodology

There are a variety of methodological designs stated in the literature [20-22] that attempt to satisfy system demands, abstraction level, model updates, and other design issues. Methods from platform-based design are used in this work. Designers are able to operate on a higher conceptual level using this approach.

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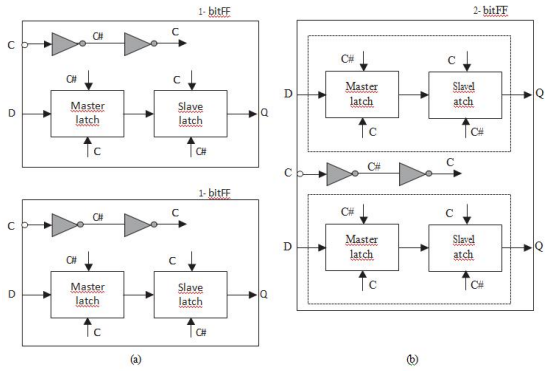

FIG4:Mergingtwo1-bitflip-flopsintoone2-bitflip-flop. (a) Before merging.(b)After merging.

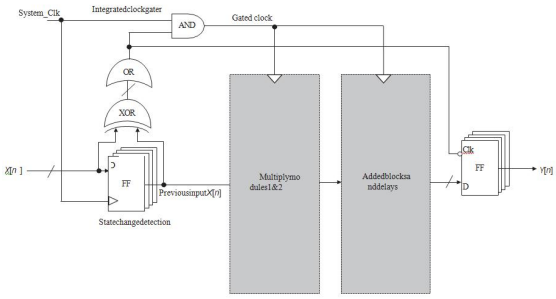

FIG5: Filter architecture with a DDCG integrated into a*k*-MBFF.

The PBD [23–26] was a method for designing products with the objectives of minimizing product lifecycle costs and increasing product reusability. This "meeting in the middle" method improves requirements while discussing abstractions of future implementations, avoiding both the bottom-up and top-down techniques. This approach eliminates the need to explicitly separate software and hardware responsibilities during system construction, allowing for building at very abstract levels. It is essential to outline not just the system's requirements and demands, but also

The designer has the freedom to choose between hardware components that can be reconfigured, hardware components that run software, or a combination of the two.

VI Results and Analysis

Using a speech signal, we have tested the proposed FIR filter. Multiple elements have been used by the current as well.

Abbreviated as "Pr," this metric compares the suggested filter's power consumption to that of the standard filter:

$$P_{\square}\left(\frac{P_{prop}}{P_{conv}}\right) \qquad (11)$$

In the parts that follow, we use the power consumption ratio as a statistic for power savings. This ratio compares the power consumption of the proposed filter to that of the conventional filter.

The proportion of power utilized due to leakage is Prl, while the ratio of power saved owing to leakage is Psl.

$$P_{sl}\square(1-P_{rl}). \qquad (12)$$

The dynamic power saving ratio P_{sd} is expressed as

$$P_{sd}\square(1-P_{rd}\quad), \qquad (13)$$

Mill watts are the unit of measurement for input power, which includes both speech

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and random impulses. The suggested FIR filter uses less electricity than the conventional version. See how the spoken input signal stacks up against the random modulation in terms of total mill watt power usage (Table 3).Total power consumption is reduced with the proposed FIR filter compared to the conventional one.

We can find the drop in filter performance by comparing the original and proposed reconfigurable filter outputs and finding the mean square error (MSE). Table 4 compares the spoken signal to the random signal using mean squared error (MSE). The MSE is reduced in comparison to conventional approaches:

TABlE1: Comparison of leakage power conception of the con- ventional and proposed FIR filters.

Filter type	Leakage power inmW			
	Random input signal		Speech input signal	
	50 taps	75 taps	50 taps	75taps
Proposed work	0.0074	0.0187	0.0059	0.00187
Reference [10]	0.0077	0.00191	0.0062	0.00191
Reference [27]	0.0089	0.00194	0.0065	0.00194
Reference [28]	0.0091	0.0096	0.0068	0.0097

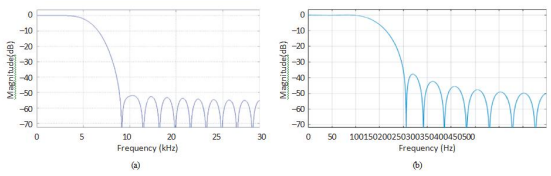
TABlE2: Comparison of dynamic power conception of the con-ventional and proposed FIR filters.

Filter type	Dynamic power inmW			
	Random input signal		Speech input signal	
	50 taps	75 taps	50 taps	75taps
Proposed work	37.8245	49.3472	52.1246	63.5862
Reference [10]	39.2663	53.1215	64.4789	76.6038
Reference [27]	43.3271	58.7612	77.6037	89.8376
Reference [28]	46.5452	64.3412	91.7230	95.5792

Figures 8(a) and 8(b) show the suggested simulation results for a low-pass FIR filter with two cut off frequencies of 100 Hz and 5 kHz. Family field-programmable gate arrays are also used to accomplish the suggested design.

TABlE3: SMR performance comparison in the speech signal case.

Filter type	Signal power to mean square error ratio(SMR)	
	50taps	75taps
Reference[32]	75.4741	86.2563
Reference[9]	75.4641	92.8273
Reference[27]	78.7937	92.1074
Reference[28]	80.1181	115.4575
Proposed work	82.5874	121.3587



A Virtex-5 platform that fits this description is the XC5VLX110T-FF136. In Table 6, we can see how much energy the suggested approach and the FIR filter utilize in contrast to one another. Table 6 shows that other design requirements, such as the amount of material resources required, are unaffected by this technique.

The proposed FIR filter minimizes power consumption, latency, and space requirements by using clock gating and multicity flip-flops. Compared to a FIR filter that relies just on one-bit flip-flops,

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this circuit is superior. Array multipliers and carry look ahead adders were used to produce the FIR filter in this design. Consider a 9-tap FIR filter; for instance, the ninth clock pulse is used to form the output. However, if you follow the suggested procedure, you should be able to get the answer on the second clock pulse. A decrease in latency and an acceleration of the circuit's performance are the final results.

Low power consumption is achieved by using multi bit flip-flops in the circuit.

The suggested method was built using the TSMC 0.25 CMOS technology as well. When running the spice-level simulations at 100 MHz using nanosim [33], we record the power usage. Energy savings and mean squared error (MSE) [5, 32] are compared in Figure 7 to earlier efforts. Compared to the filters mentioned in [5, 32], we think this one is more energy efficient.

VII CONCLUSION

The FIR filter is suggested to be redesigned in this article. The appropriate FIR filter architecture combined with DDCG and MBFFs forms the basis of the suggested design. Utilizing a voice signal and a random signal as inputs, we will compare the effectiveness of traditional and creative FIR filters. All three types of power consumption—dynamic, total, and leakage—are decreased by the suggested filter design. Using the suggested techniques, power savings of up to 22% are possible. The design's outcomes show a resource loss of less than 10%. This loss seems little due to the decrease in power use.

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