POWER-EFFICIENT RADIX-4 BOOTH MULTIPLIER UTILIZING PRE-ENCODED TECHNIQUES

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ABSTRACT: The Redundant Binary Partial Product Generator method reduces the highest height of the partial product array created by a radix 16 Modified Booth Encoded multiplier by one row. This is accomplished without affecting the latency of the block that generates the partial product. To improve the performance of binary radix-4 modified Booth recoded multipliers, we decrease the highest point of the partial product columns to [n/4] for n = 64-bit unsigned operands. The typical highest point is [(n + 1)/4], which differs from this. In this approach, the highest height is reduced by one unit. Arithmetic multipliers help the ALU and CPU perform better. The suggested approach is evaluated by comparing it to the Normal Booth Multiplier. The three areas where logic synthesis performed best were area, latency, and power. When each operand in the multiplier has a word length of 64 bits and n bits, simulations demonstrate that suggested multiplier architectures utilize significantly less space, time, and power. The proposed Xilinx 14.2 architecture is used to investigate latency and area in this study.

KEYWORDS: Modified Booth Encoding, Radix-16, Pipeline, Multiplier, Enhanced, Carry Select Adder, Binary Excess Converter.

1. INTRODUCTION

Microprocessors, digital signal processors, FIR filters, and many other high-performance digital systems rely on multipliers. There have been numerous proposals for designs and low-power multiplication algorithms that are quick.

Thanks to technological advancements, numerous researchers are currently developing multipliers for use in very large scale integration (VLSI), thanks to their consistent architecture and fast speed. When dealing with digital signals, it is essential to perform multiplication operations efficiently and rapidly while keeping the power budget in check. A simple multiplication formula is typically decomposed using three steps. One is to make partial products (pp), another is to reduce pp, and a third is to spread the end carry.

Creating a list of partial product rows is the initial step. What occurs when the multiplicand is increased by one bit is displayed in each row. The ith row of the X x Y multiplication is frequently the result of a proper left shifting of yi x X. The reason behind this is that X and Y are both represented on n bits, and the rows are structured as xn_1... x0 and yn_1... y0 in particular. Put simply, when yi equals zero, the outcome can be either a series of zeros or the multiplicand X. It is certain that in the initial phase of this example, n [1-4] PP rows were created. Forty years ago, Booth proposed the initial idea for binary number encoding. Ten years down the road, MacSorley proposed an alternative to Booth's approach. In order to reduce the amount of pp rows, a new technique known as modified booth encoding (MBE) has been developed. To a height of [n/2]+1 rows, it is capable of handling it. This is the addition of Two multiplied by itself. With radius-4, MBE creates a pp array with no additional latency, up to a height of [n/2] rows. All zeroes, +X, or +2X are the three possible values for each row in the pp array. The multiplier is able to function more rapidly as a result of this pp reduction.

Using a compression tree, all pp rows are shrunk during the pp reduction phase. This procedure produces two rows of data, known as duplicate carry save form. This allows for far quicker implementations because the intermediate addition numbers are unimportant. Display the result in a

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single row devoid of duplicates in the last addition (carry-propagated). The final addition must also contain this row. In this study, we demonstrate how to reduce the height of a pp array with up to [n/3] rows using the Radix-8 booth recoding technique. Recent results from a related study that employed a different approach to reduce the maximum height to [n/3] were encouraging . This is why the next sections will evaluate the methodology in relation to the suggested method.

2. EXISTING METHOD

The original Booth technique has been used to allay worries about sign correction in signed number multiplications even though it does not decrease the number of PPs. We have presented a modified booth encoding (MBE) method that is also referred to as the radix-4 booth algorithm. That cuts the number of PP segments in half. The parallel multiplier's complexity is greatly decreased by employing MBE. Moreover, the latency and power consumption of the complete multiplier are decreased. Assume that the multiplicand and multiplier are A = aN−1aN−2 · · · a2a1a0 and B = bN−1bN−2 · · · b2b1b0, respectively.

After the multiplier bits are encoded, groups of three neighboring bits are produced. The two side bits overlap with neighboring groups, with the exception of the first multiplier bit group. Based on the encoded results from A, the Booth decoders select -2A, -A, 0, A, or 2A to create PP rows. The multiplicand is shifted left by a conventional 1-bit to provide 2A. To perform the negation operation, flip every bit in A and add one to the position of the least significant bit (LSB). In this work, this term is called the proper term. As a result, moving or inverting the multiplicand bits makes it simple to build the PP for each line. The circuit diagram for the MBE technique is shown in Figure 2. Table 1 is an example of a basic MBE's K-Map. As a result, the Booth encoder ppij's output looks like this:

$$ppij = (b2i \oplus b2i-1)(b2i+1 \oplus aj) + (b2i \oplus b2i-1)(b2i+1 \oplus b2i)(b2i+1 \oplus aj-1) \quad (1)$$

The negation operation's corrected term is as follows:

$$Ei = b2i+1b2i + b2i+1b2i-1 \quad (2)$$

The correction term (Ei) of the negation operation is nearly identical to the multiplicative side of the multiplier, as indicated by Equation (2), with the exception of b2i+1b2ib2i−1 = 111. By reevaluating this entry in the MBE truth table, we can further reduce the complexity of Ei, it is feasible to simplify an E0 i by converting all elements in the sixth column of Table 1 to 1. Nevertheless, this would lead to a marginally more intricate pp0 ij. This is accomplished through the implementation of the subsequent methodology:

$$pp0\,ij = (b2i \oplus b2i-1)(b2i+1 \oplus aj) + (b2i \oplus b2i-1)(b2i+1 \oplus b2i)(b2i+1 \oplus aj-1) + b2i+1b2ib2i-1 \quad (3)$$

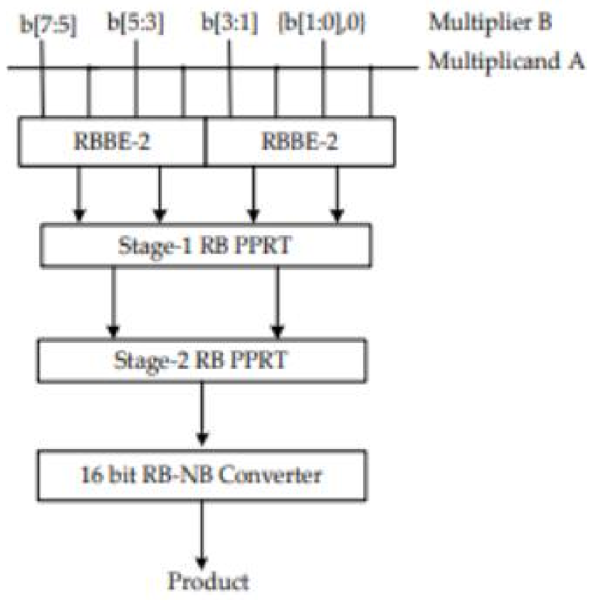


Fig. 1.The typical building blocks of an 8-bit RB multiplier

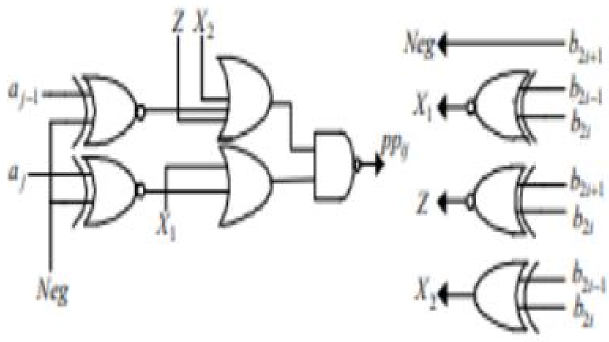


Fig. 2. MBE scheme: encoder and decoder

3. PROPOSED METHOD

The K-map of the radix-4 approximate modified Booth encoder (R4AMBE6), also known as appij6−1, is shown in Table 1. This map has six errors. When a value of 0 is present, a "1" has been changed to a "0," and when a value of 1 is present, a "0" has been changed to a "1." Only six lines need to be changed to make booth encoding easier.

The idea behind this rough design is to get the truth table to be as symmetrical as possible with as little complexity as possible. An '0' changes into a '1' in the K-map, and a '1' changes into a '0' due to three changes. The following data is made by R4AMBE6:

$$app_{ij6-1} = (b_{2i} + b_{2i-1})(b_{2i+1} \oplus a_i) \quad (17) \quad E_i = (b_{2i+1}b_{2i}) + (b_{2i+1}b_{2i-1})$$

R4AMBE6 simplifies Booth encoding and lowers critical path delay when compared to accurate MBE. The blunder rate (Pbe) is expressed as follows: Pbe is comparable to 18.75%, or 6 out of 32. Figure 5 depicts how R4AMBE6's gates are organized. Figure 2 depicts the standard MBE design. It consists of one NAND-2 gate, four XNOR-2 gates, one XOR-2 gate, one OR-3 gate, and one OR2 gate. The R4AMBE6 design requires only three gates: one XOR-2, one AND-2, and one OR-2.

Figure 1 shows the Radix-4 estimate, or app 0 ij6−1, using the new modified Booth Encoding (R4ANMBE6) with six flaws in the K-map. In this approximation design, more modifications have occurred from "0" to "1" than from "1" to "0." As a result, R4ANMB6 generally delivers more precise information than its exact counterpart.

TABLE 1: K-Map of R4AMBE6

$a_j a_{j-1}$ \ $b_{2i+1}b_{2i}b_{2i-1}$	000	001	011	010	110	111	101	100
00	0	0	0	0	1	1	1	0
01	0	0	0	0	1	1	1	0
11	0	1	1	1	0	0	0	0
10	0	1	1	1	0	0	0	0

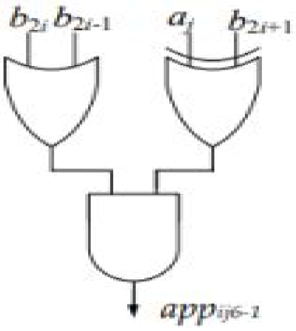


Fig. 3. The gate-level circuit R4AMBE6 that has been suggested

Table 1 is used to determine the predicted pp 0 ij:

$$app'_{ij6-1} = b_{2i+1} \oplus a_j + b_{2i}b_{2i-1} \quad (20) \quad E'_i = b_{2i+1}$$

This simplifies the comprehension of the correction term (Ei). The error rate of this one and R4AMBE6 is identical: The gate level circuit of the R4ANMBE6 is illustrated in Figure 4. The R4AMBE6 design requires only one XOR-2 gate, one AND-2 gate, and one OR-2 gate. They all require the same amount of effort.

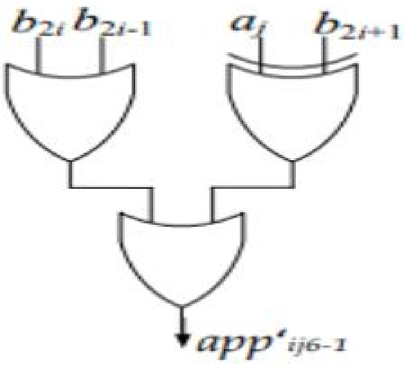


Fig. 4. This is the gate-level circuit for the R4AMBE6 that has been proposed.

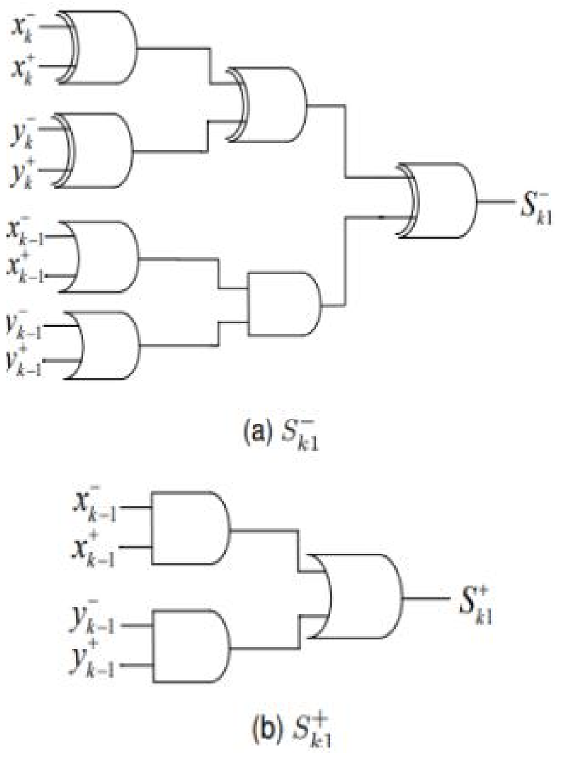


Fig. 5. The ARBC-1's gate level circuit

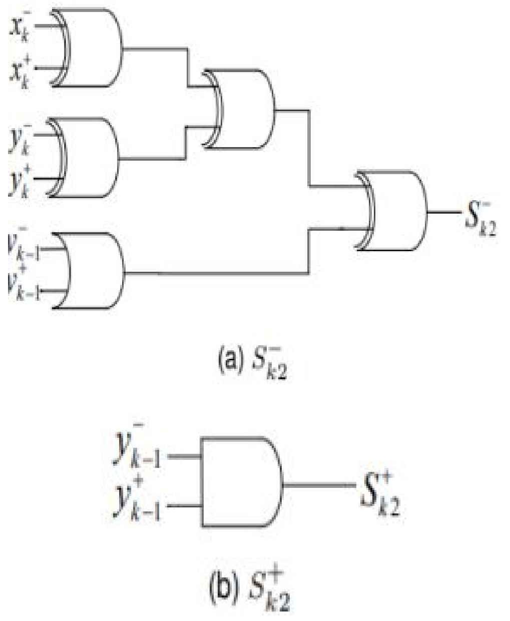


Fig.6. The gate-level circuit diagram for the ARBC-2 microprocessor.

To ensure the efficiency of designs, it is necessary to reduce the difference between the approximate RB compressor and its exact equivalent. The compression yields identical outcomes when either (1, 0) or (0, 1) is equal to (x - k, x + k). Therefore, the result stays accurate, despite the fact that the RB compressor produces a different conclusion (x − k,x + k) = (1, 0) compared to the precise compression result (x − k,x + k) = (0, 1). Therefore, the following four compression results are similar: (0, 0) = (0, 0), (0, 1) = (1, 0), (1, 0) = (0, 1) and (1, 1) = (1, 1).

A Superior RB-NB Converter for Accuracy and Precision

You can change the biased approximate results by using ARNC with lower numbers. This is because the approximate Booth encoders and approximate RB compressors usually give results that are higher than the exact results. Using an approximation adder that makes smaller outputs is part of the compensating concept. Compared tothe exact outcomes. Because of this, it is possible to make the RB-NB conversion simpler while keeping the overall

The accuracy of the estimated RB multipliers has also been improved. In Table 6, you can see the truth table for a possible close RB-NB translator. The RB-NB digit converter can be guessed by using a simple NOR gate in the way shown below: S 0 k = S + S + k + − k The approximate RB multipliers in this part are made in the following way.

The approximate Booth encoders R4AMBE6 and R4ANMBE6 are suggested as a way to make estimated PPs. The ARBC-1 and ARBC-2 are examples of close RB compressors that can greatly improve speed and cut down on compression delay when the input size is a power of two. To change the RB digit to the NB digit, the roughly RB-NB converter is used. This converter is made up of NOR gates. It works with a suggested guess factor p (where p = 1, 2,..., 2N). This is the number of least important PP columns that the approximate Booth encoders made.

TABLE 2: The Conversion of RB-NB Truth Table

RB Digit (S_k^+, S_k^-)	Carry-in(C_k)	ENB (S_k)	ANB1 (S'_{k1})	ANB2 (S'_{k2})	ANB3 (S'_{k3})
(0,0)	0	1	1	1	1
(0,0)	1	0	1	1	1
(0,1)	0	0	0	1	0
(0,1)	1	1	0	1	0
(1,0)	0	0	0	1	0
(1,0)	1	1	0	1	0
(1,1)	0	1	0	0	1
(1,1)	1	0	0	0	1

The PPs in the P column are already close, so they can be put together with an RB 4:2 expander that is also close to increase speed and greatly decrease power use. For the same reason, the approx. RB-NB converter also changes the p least significant RB digits to get to the end result. We suggest four RB factors that are close to each other. In cases where p is less than or equal to 4, they use the exact regular PP array described. In cases where p is greater than or equal to 4, they use the estimated regular PP array, in which bit pairs (E2, 0) and (E3, 1) of Fig. 4 can be left out.

All of them use the approved RB-NB converter, even though their basic designs are different. The end results can be reached with the help of the exact design for the 2N-p most important PP columns. In the p PP columns, the four RB factors change in the following ways:

1) R4AMBE6 generates the p-least significant PP columns, and ARBC-1 implements the first approximation RB multiplier's approximate PP accumulation.

2) The second approximation RB multiplier (R4ARBM2) uses R4AMBE6 to build the p least significant PP columns, and ARBC-2 is used to generate the required approximate PP accumulation.

3) R4ANMBE6 generates the p least significant PP columns and ARBC-1 executes approximate PP accumulation in the third approximation RB multiplier (R4ARBM3).

4) R4ANMBE6 generates the p least significant PP columns, and ARBC-2 is used by the fourth approximation RB multiplier (R4ARBM4) to approximate PP accumulation. By controlling the inaccuracy using the approximation factor p, reasonable precision can be used in many different contexts.

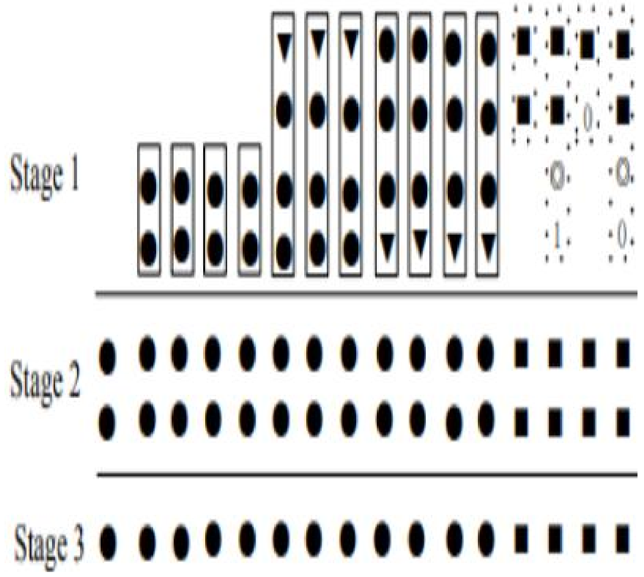
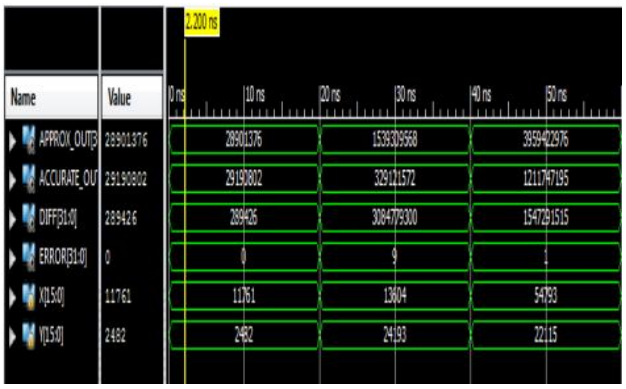


Fig. 9. The dot diagram of the 8-bit approximate RB multiplier that has been proposed

As shown in Fig. 9, an approximate RB compressor, an approximate RB-NB converter, an accurate regular PP, and an estimate Booth encoder are used to make a roughly 8-bit RB multiplier with p=4. A box with a solid line means the RB compressor is correct, while a box with a dashed line means the RB 4:2 compressor is about right. Ei stands for the expected PP term, ▼ for the changed PP after logic reduction, and ● for the real PP.

4. SIMLUATION RESULTS

Simulation is employed to evaluate and verify the functionality of the project that has been developed. The synthesis process commences with the RTL model and the Xilinx ISE utility after functional verification. The RTL model is converted into a gate level netlist and provided to a specific technology library during the synthesis phase. A diverse selection of Spartan 3E devices is included in the Xilinx ISE utility. This design was generated using the "XC3S500E" device and its accompanying "FG320" package. The device's cadence was configured to "-5." The outcomes were subjected to the subsequent analysis after this design was synthesized:



```
Name          Value      0 ns  10 ns      20 ns  30 ns        40 ns  50 ns
APPROX_OUT[3  28901376         28901376          1539309568          3959422976
ACCURATE_OU   29190802         29190802          329121572           1211747195
DIFF[31:0]    289426           289426            3084779300          1547291515
ERROR[31:0]   0                0                 9                   1
X[15:0]       11761            11761             13604               54793
Y[15:0]       2482             2482              24193               22115
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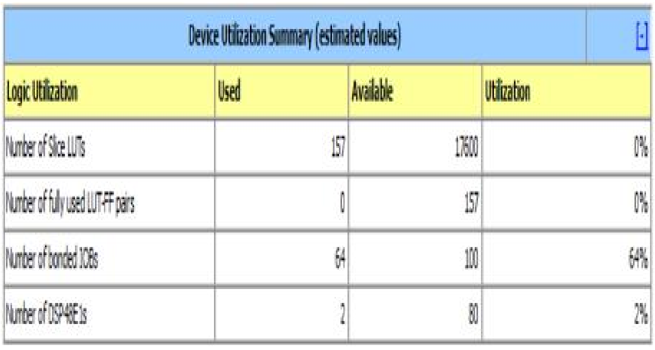
Fig 7: Simulation Result



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	157	17600	0%
Number of fully used LUT-FF pairs	0	157	0%
Number of bonded IOBs	64	100	64%
Number of DSP48E1s	2	80	2%

Fig 8: Proposed Design Summary

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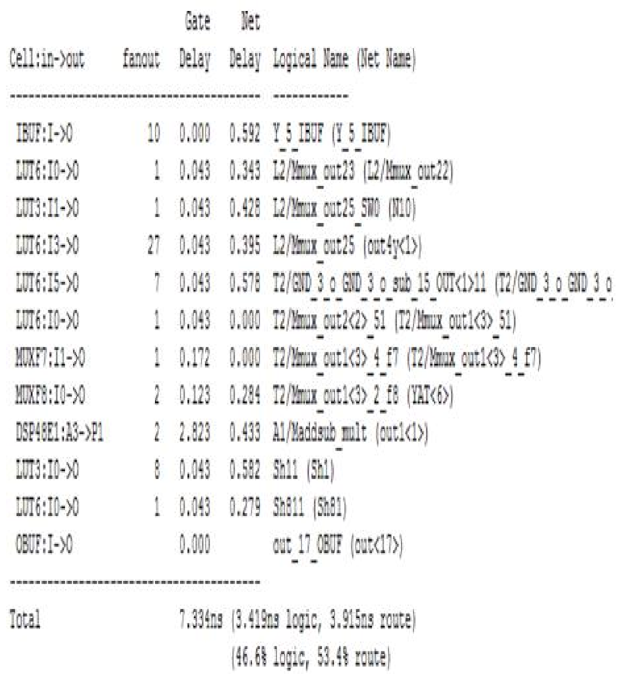

```
                           Gate    Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O            10   0.000   0.592  Y_5_IBUF (Y_5_IBUF)
 LUT6:I0->O            1   0.043   0.343  L2/Mmux_out23 (L2/Mmux_out22)
 LUT3:I1->O            1   0.043   0.428  L2/Mmux_out25_SW0 (N10)
 LUT6:I3->O           27   0.043   0.395  L2/Mmux_out25 (out4y<1>)
 LUT6:I5->O            7   0.043   0.578  T2/GND_3_o_GND_3_o_sub_15_OUT<1>11 (T2/GND_3_o_GND_3_o
 LUT6:I0->O            1   0.043   0.000  T2/Mmux_out2<2>_51 (T2/Mmux_out1<3>_51)
 MUXF7:I1->O           1   0.172   0.000  T2/Mmux_out1<3>_4_f7 (T2/Mmux_out1<3>_4_f7)
 MUXF8:I0->O           2   0.123   0.284  T2/Mmux_out1<3>_2_f8 (YAT<6>)
 DSP48E1:A3->P1        2   2.823   0.433  A1/Maddsub_mult (out1<1>)
 LUT3:I0->O            8   0.043   0.582  Sh11 (Sh1)
 LUT6:I0->O            1   0.043   0.279  Sh811 (Sh81)
 OBUF:I->O                 0.000          out_17_OBUF (out<17>)
----------------------------------------
Total                      7.334ns (3.419ns logic, 3.915ns route)
                                   (46.6% logic, 53.4% route)
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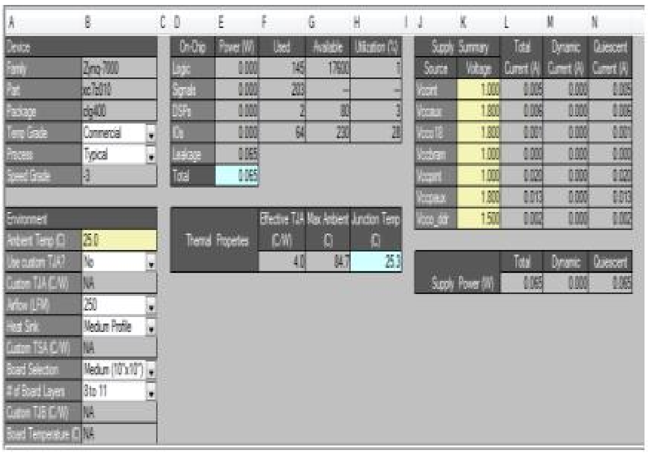
Fig 9: Proposed Timing Report



Device	
Family	Zynq-7000
Part	xc7z010
Package	clg400
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	145	17600	1
Signals	0.000	203	--	--
DSPs	0.000	2	80	3
IOs	0.000	64	230	28
Leakage	0.065			
Total	0.065			

Supply	Summary	Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.005	0.000	0.005
Vccaux	1.800	0.006	0.000	0.006
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.000	0.000	0.000
Vccpint	1.000	0.020	0.000	0.020
Vccpaux	1.800	0.013	0.000	0.013
Vcco_ddr	1.500	0.002	0.000	0.002

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.0	84.7	25.3

	Total	Dynamic	Quiescent
Supply Power (W)	0.065	0.000	0.065

Fig 10: Power Summary

Table 3: COMPARISION TABLE

	EXISTING	PROPOSED
LUTS	195	157
TIME DELAY	25.418ns	7.334ns
POWER CONSUMPTION	0.114w	0.065w

5. CONCLUSION

When compared to conventional Booth multipliers, the suggested method enhances the multiplier's power-delay product performance. We have shown how to apply a one-unit height reduction to Booth recoded magnitude multipliers with 64-bit and 128-bit radius-4. Cell-based designs with n > 32 are made possible by this decrease in latency. It may also be possible to give the reduction tree design of the pipelined multiplier more latitude. In general processors, the Booth technique that has been suggested could be quite helpful. Mobile application processors, digital signal processors, and mathematical units are used in booth encoding.

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