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DESIGN AND IMPLEMENTATION OF THE BRENT-KUNG ADDER IN THE PARALLEL PREFIX FORM OF CLA

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Abstract: *A binary adder is one of the most important digital circuits in microelectronics because data is stored as bits or binary digits. Due to the increasing demand for computing technology, the adder must operate quickly with minimal circuit area and reduced complexity. Due to its much slower binary addition and propagation delay, ripple-carry adder (RCA) can cause significant bottlenecks in the operation speed. Carry look ahead adder (CLA) eliminates this delay issue at the expense of a tremendous amount of circuit area. Due to these issues, highly capable adders must be implemented to improve the overall performance of the system with as few drawbacks as possible. In this senior design project, a fast adder known as the Brent-Kung adder (BKA) is designed in the parallel prefix form of CLA to investigate its architecture, speed, and circuit complexity. The designed adder is implemented schematically using the Verilog hardware description language on the Quartus Prime software for the electronic design automation (EDA) tool (HDL). The adder is also simulated on the Altera DE2-115 design kit's field-programmable gate array (FPGA) board. The results from simulation runs and actual hardware can be evaluated for speed comparisons between different types of adder architectures. The primary objective, which was to analyze the design of BKA, its working mechanism, and the parameters involved, has been attained.*

Keywords: *FPGA, adder, carry-lookahead adder, BrentKung adder, Verilog, Altera DE2-115.*

I. INTRODUCTION

In electronics, all registers are usually represented by binary digits or bits. The instructions used to control this data are also represented by bits. Therefore, a binary adder is very important to handle these data and instructions efficiently and accurately in an electronic machine. The most important aspect is that it must work immediately. Like the 10-number device shown below, the binary system adds numbers in a conventional way. This indicates that the additional bits from the

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previous position are needed to obtain the intended sum of the corresponding bit from the corresponding position. Due to the dimension of information and commands known today, this makes the speed of operation an adventure. Therefore, traditional binary addition is no longer applicable. Consequently, several adder architectures have been patented to address this problem. This challenge is about Brent King Adder, an Adder Architectures (BKA). In [1], a review was made between ripple-delivery adder (RCA), carry-lokahead adder (CLA), Brent-Kung adder (BKA), Ladner-Fischer adder (LFA), contribution-increment adder (CIA), contribution-select adder (CSLA), and contribution-shunt adder (CSA). Each of these adders changed to using Verilog HDL. The EDA tool used became Quartus II software. The result parameters considered are space and delay. It revealed that BKA was the least late among the programming adders while occupying a moderate position compared to other adders. RCA was cascaded and evolved in a conventional manner in [2] in comparison to parallel prefix adders including BKA, LFA, Kogge-Stone Adder (KSA), and Sklansky Adder (SKA). Each of them was created using VHDL. The implemented EDA tool became Cadence software program. The results took into account space, power consumption and shutdown parameters. It clearly turned out that BKA always exhibited low space occupation, power loss and deferral.

Another review in [3] points out the overall performance variation between different types of parallel prefix adders including BKA, KSA, LFA, SKA and Han-Carlson adder (HCA) of 8-bit, 16-bit, 32-bit and 64-bit architectures. VHDL model was selected as the design and simulation language for adders in SIM simulator, Quartus II synthesizer and Altera Cyclone IV FPGA kit. In this study article, the placement and deferral parameters were mentioned. The result of delay parameter shows that BKA requires most of the time in 8-bit, 16-bit and 64-bit modes while the remaining time is in 32-bit mode. Regarding the location parameter, BKA ranks the lowest.

Other research collected RCA, CLA, and BKA in 4-, 8-, 16-, and 32-bit formats [4]. Using Cadence EDA tool, these adders were designed and simulated using commonsense-45nm CMOS technology. Delay, power amount, and transistor range have been relevant parameters for the effects. BKA claims a clear advantage for the delay parameter as it requires the least amount of time to complete the operation even if the size is small. Furthermore, it

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showed that BKA became the advanced adder in terms of power consumption as it consumed less power than 4-bit to 32-bit addition. Finally, BKA used fewer transistors when the bit size was small, but unexpectedly increased when the bit size was large

II. LITERATURE SURVEY

M. Basir et al.[2020] In this paper, an adder and multiplier branch is compared for its implementation in a new logarithmic number system (LNS). Both the adder and the multiplier are designed using a standard high-speed integrated circuit hardware description language (Verilog) program. This allows achieving the best latency and spatial performance of the 0.18 µm CMOS LNS chip. Consequently, the most reliable configurations vary with the speed and proximity of the schemes and in some cases may be compact in space, O(n), fast in latency O(log2 n), or optimized. The software is based on constant factor adders and multipliers (FXP) that are still implemented in LNS systems. The feasibility of the scheme was tested before synthesis. The results show that the Ladner Fisher (LF) adder and the modified Baugh Wooley multiplier contribute to the fastest latency and consume the least amount of space.

K. Rahila et al. [2019] Parallel prefix adders are the most common choice for fast adders. Green adder design is usually a compromise between parameters such as locality and delay. This paper discusses the evaluation and performance of multiple parallel prefix adders based on these performance parameters and thus presents an alternative to select the most suitable adder topology for ASIC implementation. The tree adder topologies considered in this work are Coggestone, Ladner-Fisher, Brent-King and Sklansky adders. This evaluation is performed for bit widths ranging from sixteen bits to 1024 bits. Along with the evaluation of conventional tree adders, an attempt is made to observe the effect of dividing the registers into separate blocks and hence the appearance of phase-level additions and their reverberation similar to that of a wave delivery adder. Is. Over the entire range from sixteen bits to 1024 bits, the Kogge-Stone adder has satisfactory delay performance and the Brent-Kung adder has excellent locality and power performance (except for RCA). The Kogge-Stone adder has a minimum approximation delay product for small values of N, while for medium to large values of N (up to 1024 bits), the Brent-Kung adder exhibits a minimum cost.

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M. Asad et al. [2017] Recent multi-core system architectures can also have a large array of cores, typically tens to massive. Hence, they are called multi-core structures. Such systems require a green interconnection network that attempts to solve two essential problems. First, the power and space cost overhead and their impact on scalability. Second, excessive access latency due to simultaneous access of multiple cores to the same shared module. This paper presents an interconnection scheme called N-conjugate Shuffle Clusters (NCSC) based on a multi-cluster multi-core architecture to reduce the overhead of the problems just mentioned. NCSC eliminates the need for router devices and their complexity, thereby reducing power and placement costs. It re-purposed and distributed shared caches over the interconnection network to increase the probability of simultaneous access and thereby reduce access latency. Multiport Content Addressable Memory (MPCAM) is used for intra-cluster language exchange. Experimental results using four clusters and four cores each indicated that the average access delay for the write method is 1.14785 ± 0.04532 ns, which is almost the same as the write operation delay in MPCAM.

N. U. Kumar et al. [2017] The carry select adder is one of the most important adders used for arithmetic operations. It is a high-speed adder used in VLSI architecture but at the cost of space and power. Several VLSI architectures of carry select adders using the Brent-King adder are given in this paper. Experiments have been completed and simulations have been achieved using XILINX 12.2. The proposed work shows that a 16-bit carry-select adder using Brent-King adder has less on-chip space with slightly higher latency and is the fastest adder among various CSLA architectures

III. DESIGN AND IMPLEMENTATION

This step describes the design of the Brent King adder using the Verilog programming language in the Altera design environment. This section explains how to design a priority adder, BKA, using a specific EDA device in QuartusPrime software. Verilog is a specific HDL used as the programming language for this project. The FPA hardware simulation is an Altera DE2-115 design kit.

A. Electronic Design Automation

Tool The tool used for this article is called a Digital Design Automation (EDA) tool. EDA, also known as computer-aided design (ECAD), is a type of software for designing digital systems that include

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integrated circuits and printed circuit boards. The design of complex integrated circuits is enhanced, which is one of its advantages. QuartusPrime software is the EDA tool used to design the adders in this article.

As an EDA tool, Quartus Prime Lite Edition is chosen because it is efficient and ready to design complex circuits in combination with BKA. This is essential to achieve the desired effects of the designed adders. In addition, this software can be run directly on the FPGA board for hardware simulation. Although this version lacks additional functions compared to the full version, the software is still suitable and sufficient for this project dream.

B. Hardware Description Language

HDL, or Hardware Description Language, is the programming language used for Quartus Prime in this project. HDL is a specialized computer language commonly used to describe digital intelligent decision circuits and the form and behavior of digital circuits. The language is extremely easy to use which is considered as one of its advantages. Hierarchical design allows for reduction of design time, design cost, and design errors. Verilog is the HDL used to code the modules and testbench for this project.

This programming language is chosen as HDL for this project because its implementation in Quartus Prime is simple and useful. It is already an indispensable part of the EDA structure, mainly for circuits with complex designs. Therefore, this programming language is necessary for the Quartus Prime EDA device to simulate and synthesize the designed adder.

C. Altera DE2-115 Design Kit

Field Programmable Gate Arrays (FPGAs) are digital tools whose functionality can be modified. Typically, a hardware specification language is used to describe their configuration. It consists of an array of configurable common-sense blocks (CLBs) that can be interconnected using programmable interconnects. It can be reprogrammed after production to meet specific application or feature requirements. Programmable Common-Sense Components or Common-Sense Blocks of an FPGA can also encompass anything from logic gates to memory elements. It provides great flexibility.

DE2-115 is the FPGA board used for this project. It offers low cost, low power consumption, and a superior balance of intelligence, memory, and DSP capabilities. It consists of a Cyclone IV E chip, 114480 common sense elements, 3888 Kbits of onboard memory, 128 MB SDRAM, 2 MB

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SRAM, 8 MB eight-bit flash, 32 Kbits of EEPROM, 266 onboard multiplier. , three 500 MHz oscillators, 1 Gigabit Ethernet ports, and many other features. This project uses 9 LEDs as outputs and seventeen toggle switches as inputs.

D. Simulation Parameters

Task design focuses on the behavior of adders based on the mentioned parameters. The basic parameter of the adder is the speed parameter. This parameter specifies how fast the adder can achieve the desired results. In other words, the delay required by the adder to complete the addition operation for each bit must be minimized. Some adder architectures show efficient use of hardware implementations to reduce the latency problem. This creates an additional problem, which is the following: the smaller the hardware implementation, the lower the total cost and the less space occupied by the adder. There is also a circuit complexity parameter that characterizes the structure of the adder. Simplified circuits also contribute to reduced hardware implementation.

In this article, the simulation will mainly focus on the capacity of the BKA adder. One of its advantages is the ability to study speed parameters using simulation results derived from real-time gate delay waveforms. This delay is evident from the simulation results of each adder at a given time. For example, if two binary inputs are each provided within a simulation, the outputs will arrive at separate times. Therefore, their velocity parameters can be analyzed; The faster the overall overall performance, the less time it takes the adders to provide output. Since speed is one of the most important features of BKA, this work specializes in simulating its high-speed computation capabilities and comparing them with different types of adders. However, BKA is not necessarily the fastest calculator available. This is due to its structure's fan-out and depth-level issues. Fan-out indicates that a single output feeds multiple inputs, while level-of-depth refers to the layer of gates used within the structure. These parameters can be analyzed using the netlist description of the source code of the designed adders.

E. Brent-Kung Adder Module Development

The following step involves designing the Brent-Kung adder using Verilog. To make it easier to comprehend the design, simplify the code, and debug the code, modules are divided into subsections.

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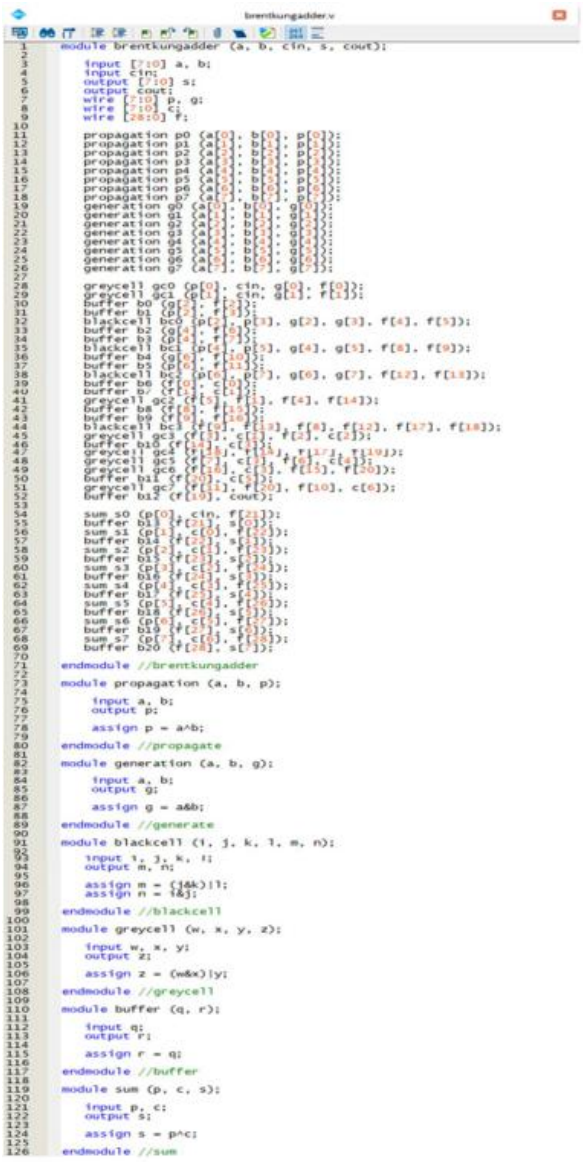

Fig.1 Implementation of Brentkungadder module

The top-level module brentkungadder is the principal module that defines the adder's architecture. The propagation and generation modules respectively calculate the propagation and generation of signals. The black cell, grey cell, and buffer modules are the logic used to generate carry signals within the carry generation stage. The summing module is the logic operation performed between the carrying and propagating signals to generate the sum bits. The modules of the BKA are described in Verilog code in Fig. 1

Test Bench

The test bench is a procedure for determining whether the designed adder behaves appropriately or not. The module is tested by assigning inputs and evaluating the resulting outputs. Verilog is also the language used to code the test bench. To begin coding the test bench, create a new text editor named brentkungadder_tb and save it. The BKA's test bench is depicted in Verilog code in Figure 5.

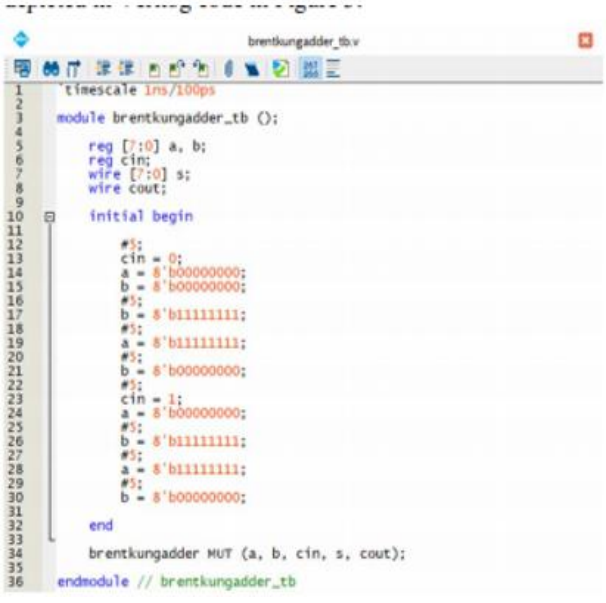

Fig.2 Implementation of brentkungadder _tb Test Bench

IV. CONCLUSION

This article discussed the design and implementation of the Brent-Kung adder on the Altera DE2-115 design kit. Various adder architectures, including ripple-carry adder, carry-lookahead adder, and Brent-Kung adder, were described. As characteristics of a parallel prefix adder, the primary parameters considered are speed and circuit complexity. There are detailed, step-by-step instructions for achieving the desired design. The language used by EDA tools to design the adder is Verilog HDL. The developed module demonstrates the BKA's architecture. Finally, the developed Verilog codes are implemented on the Altera DE2-115 FPGA board for physical and functional performance verification. It was able to correctly generate outputs based on the inputs provided. This research should be continued to investigate the BKA's parameters using the various hardware description languages, EDA tools, and FPGA kits in future studies. The outcomes can then be obtained and analyzed. Last but not least, the performance of the adder on other platforms is evaluated to identify additional information about the adder.

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