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Design of a Two-Step Low-Power and High-Speed CMOS Flash ADC Architecture

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Abstract: *Flash ADC is one of the most preferred architectures for high-speed analog-to-digital packages. The comparator is the building block of the entire structure of the analog-to- digital converter. Background noise, in comparison, is one of the crucial elements dissipating electricity. Therefore, this task aims to design and implement an 8-bit Flash ADC using a robust comparator that reduces background noise. Reducing background noise makes it possible to drive an ADC with better impedance, reducing power dissipation. This mixed-signal circuitry is designed and simulated using 180 nm CMOS technology. The 8-bit flash ADC only employs 128 comparators. The applied input clock is 80 MHz, with the input voltage ranging from 0.6 V to 1.8 V. The comparator block outputs 127 bits of thermometer code and sends them to the encoder, which exports the seven least significant bits (LSB) of the binary code. The most significant bit (MSB) is decided by only one DT comparator. The design consumes 2.81 mW of power on average.*

Keywords: *Flash ADC, MUX, encoder, CMOS ROM Encoder, Comparator*.

I. INTRODUCTION

The design of ADCs (analog-to-digital converters) has long been a neglected topic in electrical engineering due to the many applications that ADCs offer. The principal function of an ADC is to convert an analog signal, which is continuous and infinite, into a digital signal, which varies discretely concerning time. The three most essential steps in the development of signal conversion in an ADC are sampling, that is, sampling the analog input signal at a constant cost; quantization, that is, converting an infinite continuous-time

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(analog) cost into a discrete-time (digital) finite cost, which means that quantization will determine which binary phase looks closest to the sampled input rate; and encoding, i.e., converting the signal level into a binary code or digital cost. To examine how well an ADC performs, the two ideas to focus on are sample rate, which relates to how quickly the ADC converts from analog to virtual, and bit resolution, which allows you to determine how accurately an ADC converts.

There are 5 primary forms of ADC in use today [1]. Depending on the specifications or needs of the device, the design ADC will be chosen after considering its capabilities and talents. ADC SAR (Adjustable Approximation) has a balanced maximum velocity and backbone. A delta-sigma (DS) ADC delivers high dynamic performance and inherent anti-aliasing protection. The dual-slope ADC is calculated by comparing the acceleration and deceleration time (slopes). The tubed ADC is a modern ADC that is energy-saving and very fast. ADC flash is the fastest type; It features instant transfer without delay. The better the specified resolution, the larger the ADC flash and the more power-hungry it is, so the sampling rate should be reduced. Flash ADCs are used in many applications, including digital oscilloscopes, microwave measurements, optical fibres, radar detection, broadband radio, etc. [2]. According to these characteristics, ADC flash has continuously gained the most knowledge in ADC research. It is the fastest and has a simple parallel structure. These benefits make flash ADCs extraordinarily convenient and reliable in maximum builds and designs. However, while it is preferable to consider which speed is better, no one can do anything about the power consumption of high-speed devices, which should be much lower for the sake of quality performance since efficient energy outlets are needed on all devices. These items can change our location or price discount.

The flash ADC proposed in this paper includes two bulky elements: the comparator block and the encoder block. The comparison block compares the analog input and converts it to a thermometer symbol. As indicated above, there are several types of comparators whose capabilities differ from one another in terms of specifications or design requirements. This design implements a DT comparison geometry, which was commonly delivered and improved in [3]. The goal was to cut the comparator count in half compared to a traditional ADC flash. The design provided generates the maximum significant bit (MSB) at a

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switched reference voltage. With only one comparator, it was decided that MSB should be based on the input tag. This architecture also implements TIQ technology to help buy power and make the design less complex. The encoder block inputs the thermometer code sent from the comparator block and converted it into a default value as an output signal. The block encodes the thermometer code to convert it to gray code and binary code. Both blocks are designed in the 180nm CMOS era. In addition, an 8:1 analog multiplier and SPI block have been introduced to make the design more helpful even when in use. The main objective of this work is to build an 8-bit flash ADC with fewer assets compared to the conventional design to meet the needs of lower power and bandwidth area needs. This should remove the vulnerability inherent in the flash ADC. To achieve this, the ADC employs only half the comparators used in a conventional design. The DT structure of all design comparisons is achieved, considering that it is a shallow impedance structure. The design operates with a sample load of 20 to 80MHz with an input of 0.6 to 1.8V. The low power target was reached at 2.81 megawatts (eighty megahertz). The area used for coordination was 0.088 mm2, which also met the expectations of the low point. The FOM is priced right, finishing at 877.47 fJ/step. The design can be applied in small stat acquisition structures for targeted use.

II. FLASH ADC

Flash Type ADC is based on the principle of comparing analog input voltage with a set of reference voltages. To convert the analog input voltage into a digital signal of n-bit output, (2n– 1) comparators are required. It is the fastest type of ADC because the conversion is performed simultaneously through a set of comparators, hence referred as Flash type ADC.

Also called the parallel A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output. Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. An N-bit Flash ADC consists of 2N resistors and 2N –1 comparator arranged in a cascade.

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Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The 2N –1 comparator output therefore behaves in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a thermometer code. Since 2N –1 data output is not really practical, they are processed by a decoder to generate an N-bit binary output. The architecture uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high-power levels. Hence, the problems of Flash ADCs include limited resolution, high power dissipation because of the large number of high-speed comparators and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators [4].

III. LITERATURE SURVEY

In this section, we survey on different methods and applications of high-speed low power flash ADC.

George Tom Varghese and K.K. Mahapatra et al. [5] was proposed 5-bit streak ADC which is extremely effective low power encoder strategy for a gigahertz every example. In this paper, the encoder was composed in 90nm innovation with 1.2V force supply utilizing pseudo NMOS logic style to enhance the speed and reduce the power consumption furthermore decrease the bubble error which is produced because of test and hold circuit and sign delay. The normal power consumption was 0.3149mW.

Pradeep Kumar and Amit Kolhe et al. [6] introduced the outline of low power 3 bit flash ADC using 0.18 um technology with 1.3V force supply. This paper was proposed and clarified how the flash ADC is quick contrasted with other ADC structural planning furthermore clarified how it is inside codes extremely inefficient to hardware. So it is commonly just utilized as a part of uses where the latency is paramount and the hardware multifaceted nature is unassuming. The one restriction of the ADC converter is the exactness on account of simplicity of the circuits. For high resolutions the flash ADCs are very costly as a result of complexity is exponentially increments with the quantity of bits increments. The normal power consumption was 36.273 mW.

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Mamta Gurjar and Shyam Akashe et al. [7] proposed the flash ADC converter for threshold inverter quantization with low power encoder. In this paper, proposed the fast ADC converter using fat tree encoder which is exceptionally suitable and precise. The comparator was outlined using TIQ technology. The TIQ technology gives high conversion speed and makes ADC faster.

K.Lokesh Krishna and T. Ramashri et al.[8] executed the Novel hybrid analog to digital converter which contains two stage quantizer has a flash ADC and SAR ADC with resistor ladder. Actually, for rapid operation, flash ADC is utilized and for low power and high resolution, SAR ADC is utilized. By utilizing the flash ADC, we can enhance the speed and by using the SAR ADC we can accomplished the power decrease and resolution. To defeat the drawbacks, for example, low speed, hybrid ADC has been implemented. In this paper, the designed converter achieved great performance and it is suitable for high speed or high frequency applications.

Dr.A.R.Aswatha and Dr.R.Ramesh et al. [9] proposed the low power design system for flash ADC. With the assistance of this technique, we can reduce the power utilization of flash analog to digital converters when reduced the quantity of comparators by half. This paper was proposed the precision of the flash ADC by using the T/H circuit. Their proposed technique spared 35% of power consumption when contrasted and the conventional one.

Parthasarthy K.P. and, Dr. K.C.Narasimhamurthy et al. [10] proposed the usage of the low power consumption flash ADC for very high end receivers. The demanding issue in this paper was to design a low power latched comparator using 90nm technology with 0.8V DC supply. This technique consumes low power of 7.67mW, which consumes a low power of around half for a sampling frequency upto 1.2GHz. This configuration can be extended to high-speed applications because comparator utilized as a part of this plan can work upto 5GS/s.

Kirankumar Lad and M.S.Bhat et al. [11] planned the flash ADC which accomplishes 5.76 ENOB at nyquist input frequency without adjustment. The INL and DNL are 0.08LSB and 0.1LSB individually. This technique consumes low power of 15.75mW with 1V supply and an energy efficiency is 0.29pJ/conv working at 1GS/s.

R Komar et al. [12] proposed a 0.5 V, 50 MS/s, 6-bit Flash ADC with 180 nm CMOS technology. In this design an inverter-based comparator is used to

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reduce the silicon area and power necessity for a high low voltage operation low limit MOSFETs are used. For expanding the power effectiveness and speed of operation, a basic clock deferring technique and consecutive inverters in the comparators have been used. For digitizing comparator yields, A fat tree encoder design is used. The SNDR is 31dB for the input frequency of 5. 1MHz.The INL and DNL are 0.375LSB and 0.025LSB separately and power consumption is 0.3mW

IV. DESIGN AND IMPLEMENTATION

An overview block diagram of this 8-bit flash ADC is presented in Figure 1. The 8:1 analog multiplexer (MUX) selects between 8 analog inputs. Then, the selected analog signal A_OUT is sent to two main blocks—the comparator block and the encoder. The MSB of the 8 binary bits, Q [7], is decided right after the analog input A_IN passes through a DT comparator. The remaining output bits, Q[6:0], are decided by the thermometer code T[127:1] generated by the Comparator block and then goes through the Thermo-to-Gray-to-Binary Encoder. To make the design more convenient for testing and use, we attach an SPI block that works as an enslaved person. This would help the ADC transfer digital data adequately

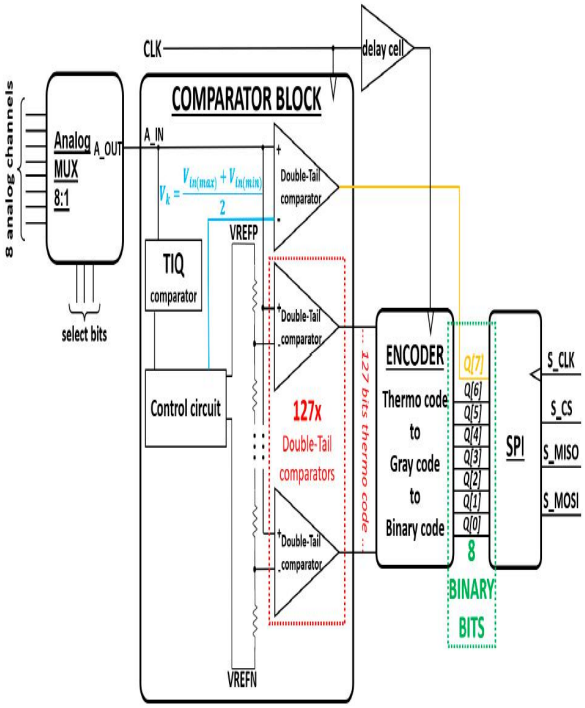

Fig.1 Block diagram of this 8-bit flash ADC

Figure 1 provides the schematic view of the 8:1 analog MUX. This MUX has 8 input channels which are 8 analog signals. There are 3 bits used for channel selection. Depending on these 3 bits, 1 of 8 analog signals will be picked and sent to the Comparator block. Each input line is followed by 3 serially connected NMOSs and 3 serially connected PMOSs. Each selection bit is divided into two separate lines with opposite logic (by passing through an inverter). Specific conditions with corresponding outputs of this MUX are presented in table.1

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Table.1 The truth table of the 8:1 analog Mux

SEL2	SEL1	SEL0	OU
0	0	0	IN
0	0	1	IN
0	1	0	IN
0	1	1	IN
1	0	0	IN
1	0	1	IN
1	1	0	IN
1	1	1	IN

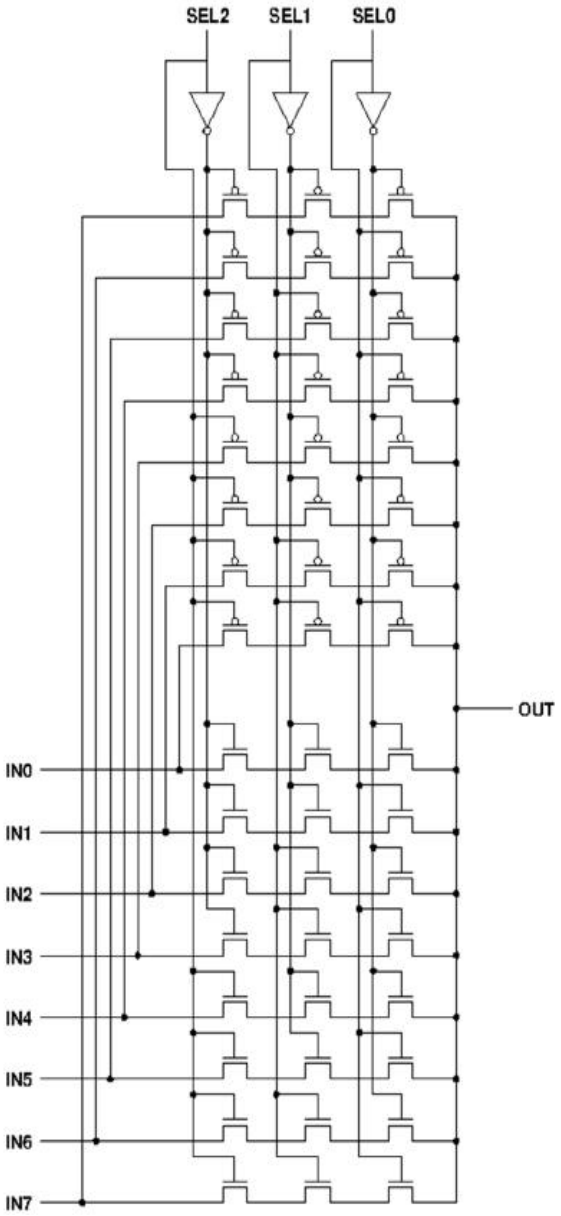

Fig.2 The 8:1 analog Mux

Comparator Block

In a flash ADC, the most significant part is the Comparator block. Requirements should be met regarding power and resource-saving but must make sure the ADC works a high speed. After researching various types of comparator architecture, it was decided that this paper would follow the comparator structure presented in [13]. A general view of a full N-bit flash ADC is suggested in Figure

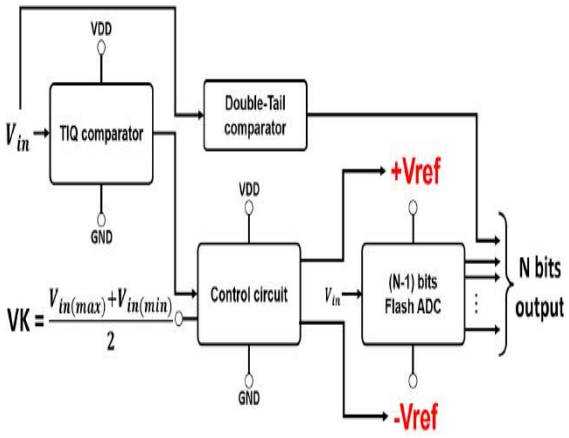

Fig.3 The proposed architecture of N-bit flash ADC

As we can see, the leverage given by this architecture savis resources by reducing the number of comparators by half. For instance, conventional N-bit flash ADC requires 2^{N-1} comparators. However, this structure only needs 2^{N-1}.

V. SIMULATION RESULTS

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The proposed ADC architecture is designed and implemented using two-stage open-loop comparator with 180 nm CMOS technology. The simulations are carried out using the commercially available cadence tool. The performance of the designed control circuit is analysed by using the transient analysis. Here, the control input is considered as a clock pulse with a voltage range of -1.8 V to 1.8 V. The VTC curve of a control circuit confirms that the switching of reference voltages between +Vref (+1.8 V) and Vref (-1.8 V) around midpoint voltage VK (0 V) as shown in "Fig. 9". The comparator generates an appropriate control input with respect to the input signal.

A) Analog MUX

We can look at the analog mux functionality for good measure by utilizing 8 unique analog alerts and moving through the selector bits through 8 cool conditions. The test provides eight sine waves of the same amplitude but exclusive frequencies from 1 to 8 kHz. The 8:1 analog MUX deployment layout simulation result is verified in Figure 9

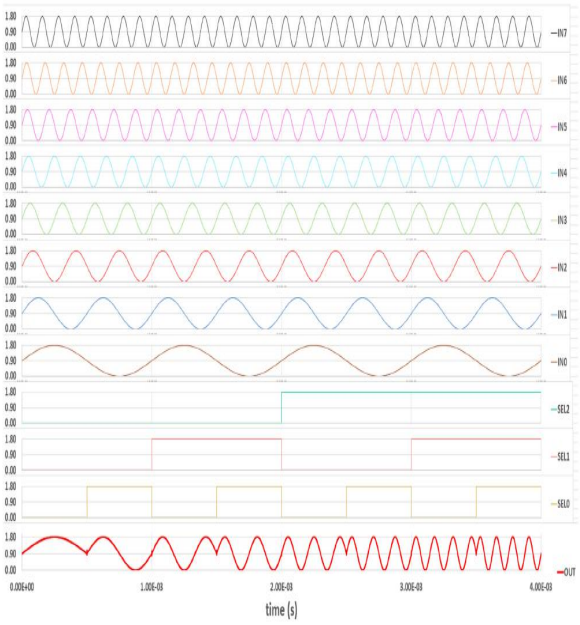

Fig.4 The 8:1 analog MUX post-layout simulation

B) Comparator Block

TIQ Comparator

The TIQ comparison is simulated in the DC rating as the input signal IN steps from 0.6 Vdc to 1.8 Vdc. The output results are shown in Figure 10. By adjusting the sizes of the transistors, the edge voltage Vth can be determined as expected. The ideal condition is that the output voltage satisfies the input at half the input voltage range, V = 1.2 volts.

Control Circuit

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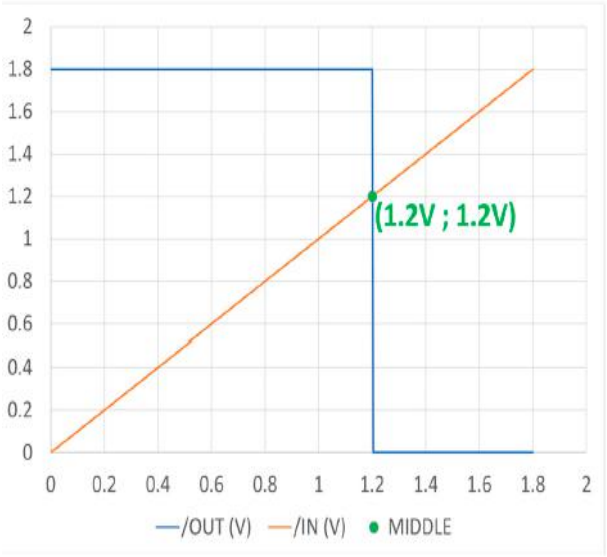

Fig.5 TIQ comparator post-layout simulation (DC)

Control Circuit

The control circuit uses pairs of similar transformers. Therefore, the edge level should be ensured for these investors, as we did earlier with the TIQ comparison. The result of the simulation here now does not include weight (resistance ladder) to reveal later within the entire device. The load reduces the output reference voltages, so additional M11 and M12 devices are provided to bring this number back to normal, as shown in Figure 11a. The input condition is that IN varies from 1.8 to 0.6 VDC. As we will examine, the VCTRL output of the TIQ comparison above changes at the 1.2-volt midpoint from zero V to one. -VREF] is [1.2V; 1.8 volts]. When IN is less than 1.2V, [+VREF; -VREF] is [0.6V; 1.2 volts]. Figure 11b shows the result of the DC simulation, which presents the voltage switching characteristic (VTC) curve. This way, the reference voltages +VREF and -VREF are transmitted about half a factor of the 1.2 VDC voltage.

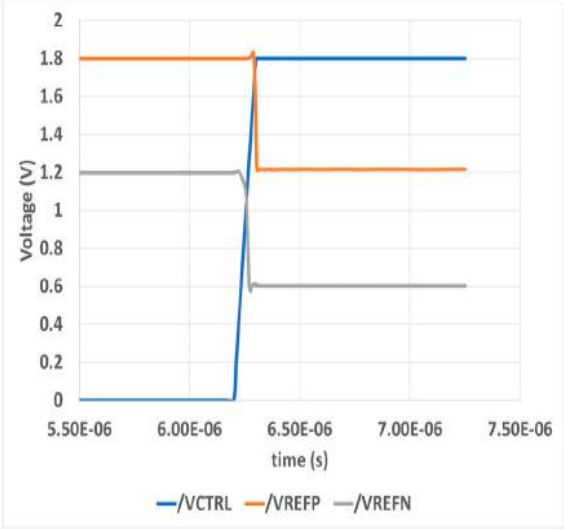

Fig.6 Control circuit post-layout simulation: (a) transient analysis

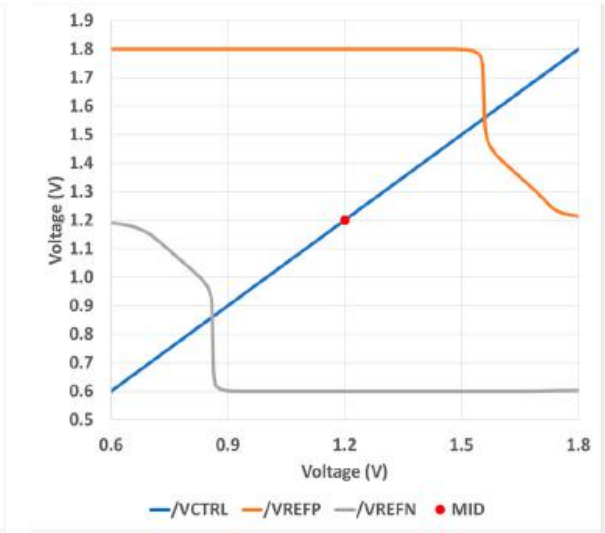

Fig.6 b) DC Analysis

VI. CONCLUSION

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In conclusion, the paper has introduced a low-power and low-area 8-bit flash ADC in the 180nm CMOS era. The design consumes an average of 2.81 megawatts of energy. The total layout area is zero, 088 mm2. The FOM provides 877.47 fJ/step. The ADC is simulated and alerts at 20MHz and 80MHz clock signals. The convertible input voltage changed from 0.6V to 1.8V. The design consists of two main useful blocks, the comparator block, and the encoder. The comparator block takes advantage of the DT comparator circuit structure with low processing time as the basis. At the same time, it is spatially more efficient while using the best DT comparator circuit to select the MSB of the binary output. This halves the number of comparator circuits compared to a conventional flash ADC. In addition, the design achieves low energy requirements thanks to the optimization of the surrounding environment. The encoder uses a structure that converts from a thermometer symbol to a medium gray code before switching to binary code output.

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