

## **A 5-level High Efficiency Low Cost Hybrid Neutral Point Clamped Transformerless Inverter for Grid Connected Photovoltaic Application**

T.RAMANJANEYULU <sup>1</sup>, SK . SALEEM <sup>2</sup>, K. KISHORE BABU <sup>3</sup>

<sup>1</sup> Assistant Professor, <sup>2</sup> Associate Professor, <sup>3</sup> Associate professor  
Department of Electrical and Electronics Engineering  
Priyadarshini Institute of Technology & Science, Tenali, Guntur

Abstract—With the increase in the level of solar energy integration into the power grid, there arises a need for highly efficient multilevel transformerless grid connected inverter which is able to inject more power into the grid. In this paper, a novel 5-level Hybrid Neutral Point Clamped transformerless inverter topology is proposed which has no inherent ground leakage current. The proposed inverter is analyzed in detail and its switching pattern to generate multilevel output is discussed. The proposed inverter is compared with some popular transformerless inverter topologies. Simulations and experiments results confirm the feasibility and good performance of the proposed inverter.

### **I. INTRODUCTION**

Over the years, solar photovoltaic (PV) energy has stood out to be an attractive solution for global energy crisis. Advances in highly efficient PV module fabrication

technologies have made the dream of rooftop solar energy a reality today. Due to their low cost and high efficiency, transformerless inverters are usually preferred to integrate the solar energy into the power grid. However, the inherent demerit of the transformerless inverters is the presence of galvanic connection between the grid and the PV array. This can lead to high ground leakage current, thereby compromising the safety of the overall system [1, 2]. The magnitude of these leakage currents between the PV panel terminals and ground depends mostly on the value of this stray capacitance and the amplitude and frequency content of the common-mode voltage variations that are present at the PV panel terminals [4]. This has led to the development of several new transformerless inverters, which employ various methods to suppress this leakage current [2, 6]. The inverters like the H5 and HERIC inverter employ decoupling methods

during the freewheeling period [2]. Another method is to clamp the inverter to the midpoint of the DC link during the freewheeling period [2]. Recently, a new inverter topology is proposed wherein; the leakage current is eliminated by connecting the grid neutral point directly to the PV negative terminal, thereby bypassing the PV stray capacitance[13]. These available transformerless inverters output maximum power in the range of few kW. Therefore, in order to output even higher power, there arises a need for a multilevel transformerless inverter which is devoid of ground leakage currents. Full bridge based transformerless inverters can never truly eliminate the leakage current due to the virtue of its topological properties[4]. Moreover, a multilevel full bridge based transformerless inverter can lead to very high leakage currents. Hence, half bridge based transformerless inverters, like the diode clamped multilevel inverter, are preferred for high power systems as they clamp the grid neutral point directly to the midpoint of the dc link, this can be seen in Fig. 1. A multilevel diode clamped inverter was proposed in [5], wherein across the individual dc link capacitors, multiple PV arrays are connected and are controlled

independently. However, as the output voltage level increases, the total inverter cost increases, whereas the efficiency of the inverter reduces. Therefore, there is a need for a high efficiency low cost multi-level transformerless inverter. In this paper, a novel 5-level hybrid neutral point clamped transformerless inverter is proposed, which attempts to provide a solution for the need of high efficiency, high power multilevel inverter.

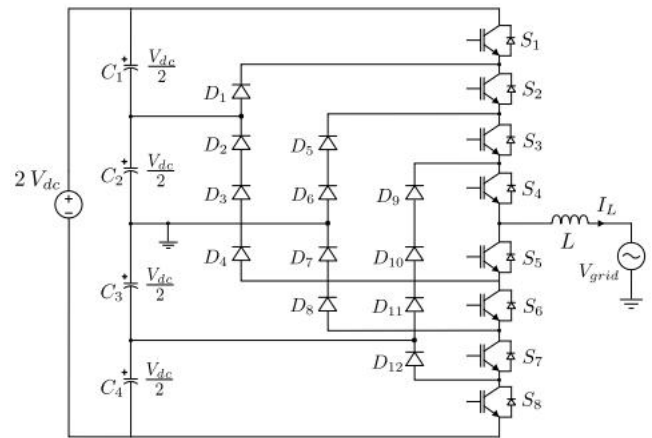


Fig. 1. 5-level diode clamped multilevel inverter

## II. PROPOSED 5-LEVEL HYBRID NEUTRAL POINT CLAMPED INVERTER

The proposed 5-level hybrid neutral point clamped (5LHNPC) inverter consists of 8 switches S1-S8, four diodes D1-D4 and four

DC link capacitors C1-C4 as shown in Fig. 2 [8].

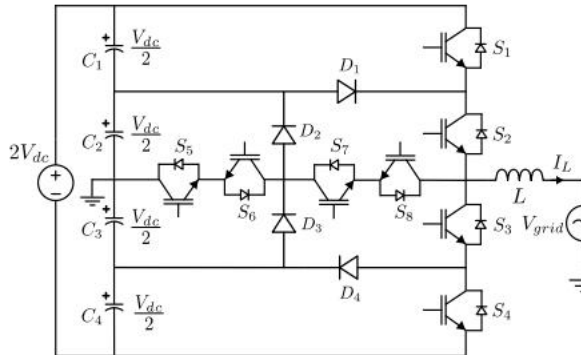


Fig. 2. Proposed hybrid neutral point clamped inverter

There are two structures, which can be employed for grid-connected PV inverters with the proposed 5L-HNPC: multistring structure and multi PV array structure as in [5], where across the individual DC link capacitors, multiple PV arrays are connected and are controlled independently. In case of multistring structure, addition chopper circuitry [9] is required to balance the DC link capacitors. In case of multi-array structure [5], the DC link voltages are balanced with appropriate control technique as each of the capacitor is connected directly to PV arrays. In the proposed topology, for a DC link voltage of  $2V_{dc}$ , the output voltages obtained are  $V_{dc}$ ,  $V_{dc}/2$ ,  $0$ ,  $-V_{dc}/2$  and  $-V_{dc}$ . The switching patterns to generate

appropriate voltages is shown in Table I. The current direction is as shown in Fig. 2. The + and - symbols in Table I represent the positive and negative current directions respectively. The proposed 5L-HNPC inverter is simulated in MATLAB Simulink and the results for output voltage and current are shown in Fig. 3.

TABLE I  
SWITCHING PATTERN TO GENERATE 5-LEVEL OUTPUT

$V_o$	$S_1$	$S_2$	$S_3$	$S_4$	$S_5 / S_6$	$S_7 / S_8$	$I_L$
$V_{dc}$	1	1	0	0	0	0	+/-
$V_{dc}/2$	0	1	0	0	0	0	+
$V_{dc}/2$	0	0	0	0	0	1	-
0	0	0	0	0	1	1	+/-
$-V_{dc}/2$	0	0	0	0	0	1	+
$-V_{dc}/2$	0	0	1	0	0	0	-
$-V_{dc}$	0	0	1	1	0	0	+/-

The comparison between the proposed inverter and the conventional 5-level diode clamped inverter (5L-DCMLI) is shown in Table II. Here the devices  $S_2$  and  $S_3$  are rated for  $3V_{dc}/2$ ,  $S_1$ ,  $S_4$ ,  $S_5$ ,  $S_6$ ,  $S_7$ ,  $S_8$ ,  $D_1$  and  $D_4$  are rated

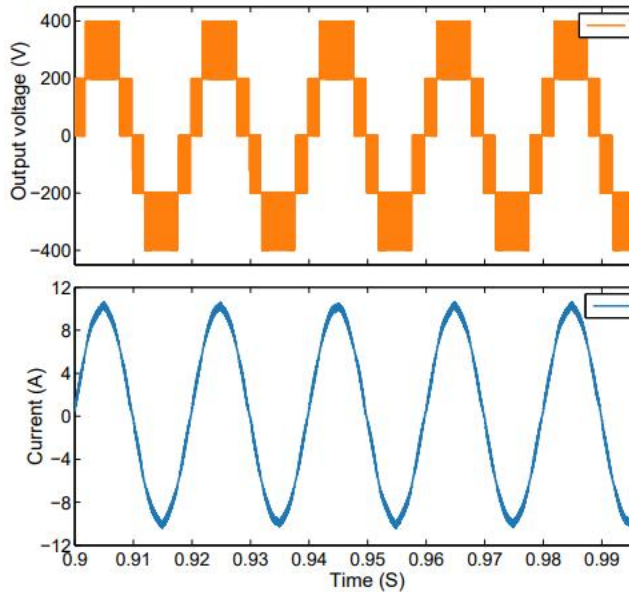


Fig. 3. Simulation results for 5L-HNPC

for  $V_{dc}/2$  and D2 and D3 are rated for  $V_{dc}$ , which makes total of 18 semiconductor devices each rated for  $V_{dc}/2$ . The conventional 5L-DCMLI shown in Fig. 1 has 8 switches and 12 diodes each rated for  $V_{dc}/2$ , which makes total of 20 semiconductor devices. Therefore, the proposed inverter needs two fewer devices as compared to 5L-DCMLI. The proposed inverter needs only 6 identical diodes as compared to 12 diodes needed for 5L-DCMLI. Therefore, the proposed topology is subjected to lower reverse recovery loss as compared to the 5L-DCMLI. The output voltage of a single phase transformerless inverter is generally in the range of 110-250 V [2]. Therefore, instead of 12 identical

switches each rated for  $V_{dc}/2$  (200 V), only 8 IGBT switches, as shown in Fig. 2, can be used. This further reduces the switch count, thereby reducing the overall inverter cost.

TABLE II COMPARISON OF 5L-HNPC WITH 5L-DCMLI

Parameters (DC link = $2V_{dc}$ )	5L-HNPC
Number of clamping diodes	4
Total voltage rating of diodes	$3V_{dc}$
Maximum voltage rating of diodes	$V_{dc}$
Number of switching devices	8
Total voltage rating of switching devices	$6V_{dc}$
Maximum voltage rating of switching devices	$1.5V_{dc}$
Number of DC link capacitors	4

### III. LOSSES AND EFFICIENCY ASSESSMENT

The standout feature of transformerless grid connected PV inverters is its low cost and high efficiency. To have a fair and accurate efficiency comparison of the proposed inverter with the conventional transformerless inverters, the losses and efficiency estimation is carried out considering same devices and circuit parameters for all the inverters. Also, the efficiencies at different output power levels is evaluated

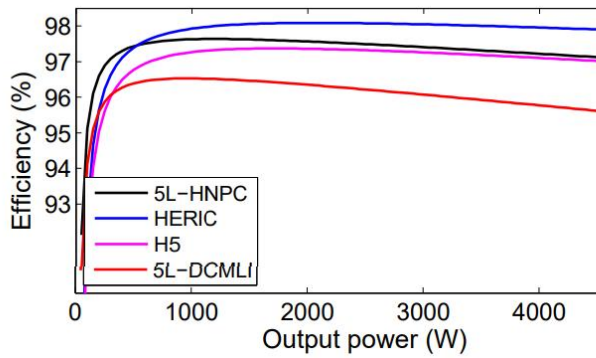


Fig. 4. Efficiency curves of various inverters in order to compare weighted efficiency of these topologies. In order to calculate device conduction loss, the first order voltage drop model [11] of the devices is used as given by (1). Where  $V_t$  is the device equivalent voltage drop at no load,  $R_c$  is the device on state resistance,  $i(t)$  is the load current expressed as  $i(t)=I_m \sin(\omega t)$  and  $I_m$  is the amplitude of the load current

$$v(t) = V_t + i(t) * R_c$$

The duty ratios for active and zero stage is given by  $D_a$  and  $D_z$  respectively. where  $m$  is the inverter modulation index and  $\omega$  is the grid frequency in radians.

$$D_a = m * \sin(\omega t)$$

$$D_z = 1 - m * \sin(\omega t)$$

$$P_{cond} = \frac{1}{2\pi} \int_0^\pi v(t)i(t)D(t) d\omega t$$

As the PV inverters usually operate at unity power factor (UPF) [2], the device conduction losses of the proposed 5LHNPC inverter are calculated at UPF and for a modulation index of 1. From (1), (2), (3) and (4) we have the device conduction losses as listed below.

$$P_{S1} = P_{S4} = 0.2356 * V_t * I_m + 0.2067 * I_m^2 * R_c$$

$$P_{S2} = P_{S3} = 0.29 * V_t * I_m + 0.241 * I_m^2 * R_c$$

$$P_{S5} = P_{S6} = 0.0282 * V_t * I_m + 0.009 * I_m^2 * R_c$$

$$P_{S7} = P_{S8} = 0.0282 * V_t * I_m + 0.009 * I_m^2 * R_c$$

Similar loss calculation is performed for 5L-DCMLI and other popular transformerless inverters like H5 and HERIC inverters. For loss calculation the IGBT characteristics of SKM 50GB12T4 [12] operating at 12 kHz is considered. The efficiency curves of the various inverters are shown in Fig. 4. The weighted CEC efficiency of the proposed 5L-HNPC, 5L-DCMLI, H5 and HERIC inverter is 97.37%, 96.03%, 97.18% and 97.97% respectively. Therefore, it is evident that the efficiency of proposed inverter is

comparable to that of HERIC inverter and significantly higher than that of 5L-DCMLI. This is due to the fact that, for a 5L-DCMLI, 4 devices conduct during the active output voltage states of  $V_{dc}$ ,  $0.5V_{dc}$ ,  $-0.5V_{dc}$  and  $-V_{dc}$ , whereas, for the proposed 5LHNPC only 2 devices conduct during those active voltage states. For the proposed inverter, as the output voltage is of 5 level, zero voltage state occurs only during  $120^\circ$  period of the total cycle. Moreover, for UPF operation, during this  $120^\circ$  period, the current magnitude is low as the current wave goes through zero crossing. Therefore, although 4 devices conduct during the zero voltage state, the proposed inverter has lower losses as compared to 5L-DCMLI.

#### IV. EXPERIMENTAL VERIFICATION

To validate the operation of the proposed topology, a laboratory prototype of the 5L-HNPC inverter is built as seen in Fig. 5. The SKYPER 32R gate driver is used to drive IGBT modules SKM-50GB-12T4. For the neutral point clamped inverters like the conventional diode clamped inverter, the balancing of dc link capacitors needs special attention. There are several methods which can be used to balance the dc link capacitors like using a suitable modulation strategy or

using a chopper balancing circuit [9] etc. These methods can also be used to balance the dc link capacitors of the proposed inverter. For testing out the laboratory prototype of the proposed inverter, a dc link of 120V is realized using a regulated power supply and a chopper balancing circuit as described in [9]. This can be seen in Fig. 6.

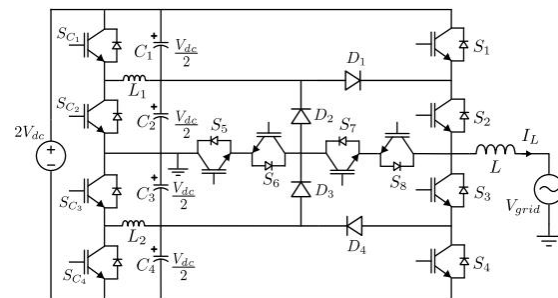


Fig. 6. Proposed 5L-HNPC with chopper balancing circuit

The system hardware configuration is shown in Fig. 7. The control signals for the inverter are generated using TI's TMS320f28335 experimenter kit operating with a clock frequency of 150 MHz and sampling interval of 10s. Fig. 8 and Fig. 9 shows the output voltage and current waveforms for inverter operation at UPF and  $30^\circ$  lag respectively, thereby confirming the proposed inverter's ability to exchange reactive power with the grid.

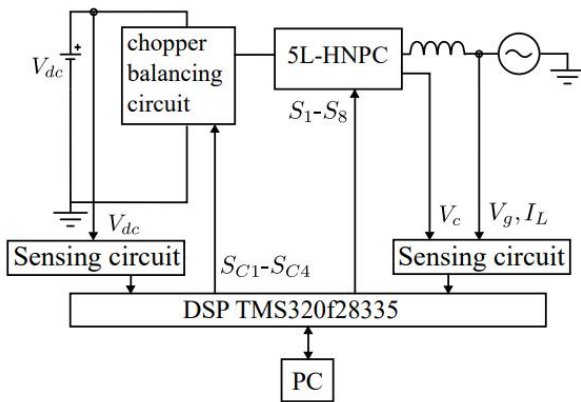


Fig. 7. System hardware configuration

Fig. 10 exhibits the dynamic performance of the inverter for a change in modulation index from 0.45 to 0.95, Fig.11 exhibits the dynamic performance of the inverter for a change in modulation index from 0.95 to 0.45. Fig. 12 and Fig.13 exhibits the dynamic performance of the inverter for a change in load. It can be seen from Fig. 14 that when

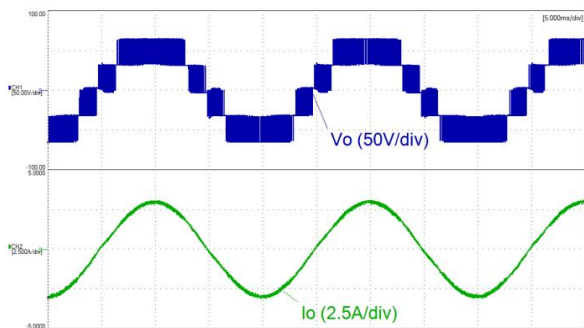


Fig. 8. Inverter operation at UPF

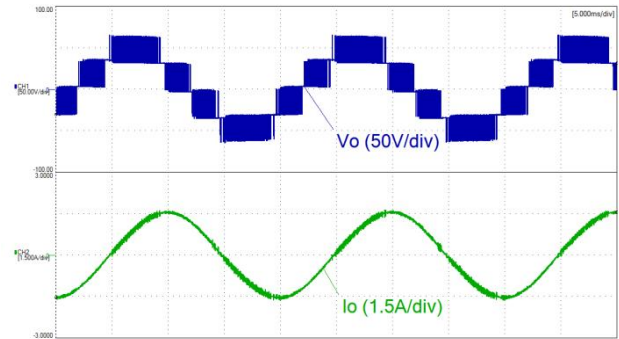


Fig. 9. Inverter operation at 30° lag PF

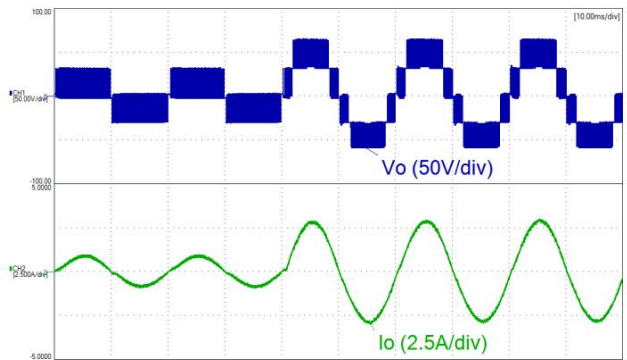


Fig. 10. Inverter output for increase of modulation index from 0.45 to 0.95

the chopper circuit is deactivated, the voltages across C1 and C2 deviate from each other in a similar way as in the conventional 5L-DCMLI. Fig. 15 shows that the capacitor

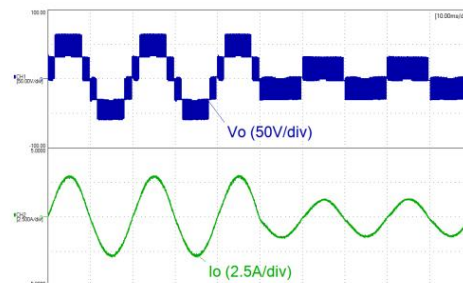


Fig. 11. Inverter output for decrease of modulation index from 0.95 to 0.45

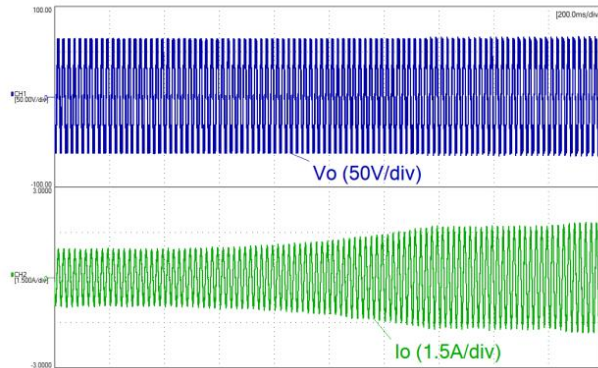


Fig. 12. Dynamic performance of inverter for increase of load

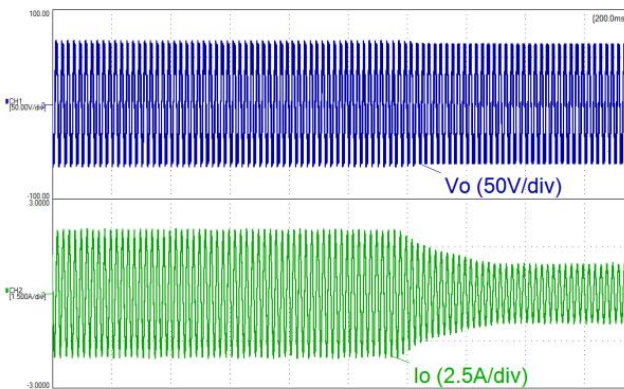


Fig. 13. Dynamic performance of inverter for decrease of load

voltages are balanced when the chopper circuit is active. The output current THD is about 1.9%, which meets the IEEE 519 standards.

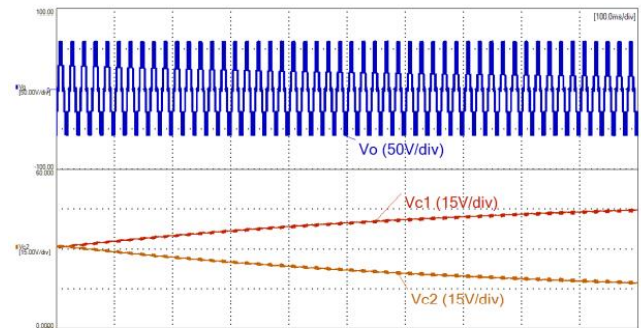


Fig. 14. Inverter operation with chopper balancing circuit activated

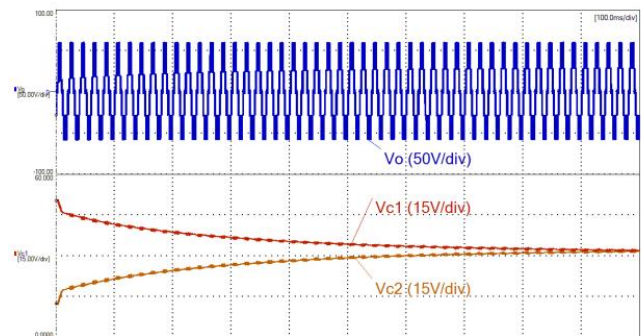


Fig. 15. Inverter operation with chopper balancing circuit deactivated

## V. CONCLUSION

A 5-level Hybrid neutral point clamped transformerless PV grid connected inverter is presented in this paper. The main characteristics of proposed transformerless inverter are: 1) Lower stress on the grid interfacing inductor, thereby reducing the filtering cost and size as compared to conventional 3-level inverters like H5 and HERIC inverter. 2) Lower cost as compared



to 5L-DCMLI as the proposed inverter requires less no of clamping diodes. 3) Higher power handling capability as compared to conventional 3-level inverters. 4) Higher efficiency as compared to 5L-DCMLI and H5 inverter. 5) No common mode leakage current as the proposed inverter belongs to the family of half bridge inverters. 6) The proposed inverter is capable of exchanging reactive power with the grid. Therefore, with excellent performance in eliminating the CM current, multilevel output voltage and high efficiency, the proposed inverter provides an exciting alternative to the conventional transformerless grid-connected PV inverters. Moreover, due to its superiority over the 5L-DCMLI in terms of efficiency and cost parameters, the pertinence of the proposed inverter is not limited to grid connected PV inverters and it can find its way for all the applications where currently 5L-DCMLI are employed.

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