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# Design and implementation of memory unit by using 8T-TG DTMOS based SRAM cell

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***Abstract***: *Recently, the demand for portable communications has led to more and lower power ASIC (Application Specific Integrated Circuit) designs. It has been shown that power consumed during memory accesses accounts for a significant portion of the total power consumption in microprocessors, thus minimization of memory was as an important area of concern for today's IC designers. A new design contains transmission gate as an access transistor. Simulation results of power dissipation, access time, current leakage, stability and power delay product of the proposed SRAM cell have been determined and compared with those of some other existing models of SRAM cell.*

*Keywords: Subthreshold SRAM Cell, Power Delay Product,8T cell, low power.*

## I. INTRODUCTION

Some virtualization applications require systems with much lower power consumption without compromising reliability. Virtual battery-powered structures make it more convenient to have a battery of short length, as it accounts for most of the device's weight. However, a smaller battery means less electricity is saved. Therefore, to get an accurate standby time with a smaller battery, it must also reduce the power fed with the help of the system. This has caused an additional focus on reducing the power consumption of today's digital circuits. We aim to design a mobile SRAM capable of operating at a lower connection voltage to reduce power consumption. However, this type of design inevitably leads to a cell with a larger area or higher delay than a conventional SRAM cell. While there are many strategies for reducing the power input in virtual circuits, the most significant reduction is achieved by

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lowering the conduction voltage. When the conduction voltage decreases, the dynamic power consumption decreases quadratically [1], and the input leakage power decreases linearly [2]. As the conduction voltage tends toward the transistor's limiting voltage, margins of virtual circuit noise deteriorate into unacceptable ranges. As a result, the digital circuit begins to fail. Also, at lower voltages, the device delay time is significantly prolonged due to the smaller currents through the circuit.

Based on the type of load used in a Flip-Flop inverter, SRAM cells are categorized into three categories: the 4-cell transistor, 6-transistor cells, and Thin Film Transistor (TFT) cells. Of these 3 types, 6 SRAM transistors are the most widely used. SRAM cells keep records as long as power is supplied and lose their stored data once power is removed. It does not require periodic refresh operations like DRAM because SRAM statistics are stored in a flip-flop rather than a capacitor. The static RAM cell in the statistical garage includes a latch circuit that typically stores 1-bit registers, and the mobile memory consists of two hardpoints at nodes A and B, as shown in figure.1

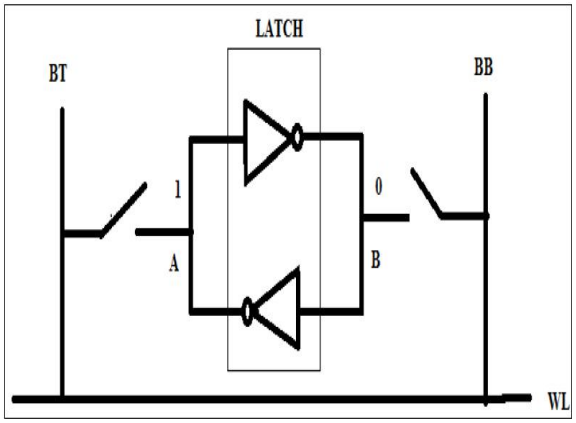


**Fig.1**Basic SRAM cell

The word line is used to access data stored in the mobile phone's memory through complementary bit lines. Bypass data is saved in bit traces if you want to improve overall memory performance by estimating noise immunity and performance.

The conventional SRAM 6T rover shown in Figure 2 includes a pair of dual step-down shifters and access transistors. Direct access transistors (N3 and N4) connect tracer bits (BL and BLB) to data storage nodes (Q and QB). They are controlled using a Word Line (WL), which runs along the chip horizontally, simultaneously controlling access to the transistors of different cells in the same row. Bit lines are sometimes called register lines because they bring data in and out of the cell. The bit voltages are preloaded to the VDD, and the WL is pulled out quite a bit to perform the test process. The bit line associated with the node that stores the '0' is discharged by reaching up to the transistor

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and pulling it down. During the writing process, the statistics to be written to the handheld device are executed in bit traces, and then the WL line is overdrawn. When the rover is not studied or written, the WL is pushed to GND to separate the bit traces and garage nodes. However, the traditional 6T SRAM mobile does not

It works properly when the supply voltage drops to zero., 5V. The write potential of the cell is low at this supply voltage [2]; furthermore, due to the low read current, the read access time of the cell is high.

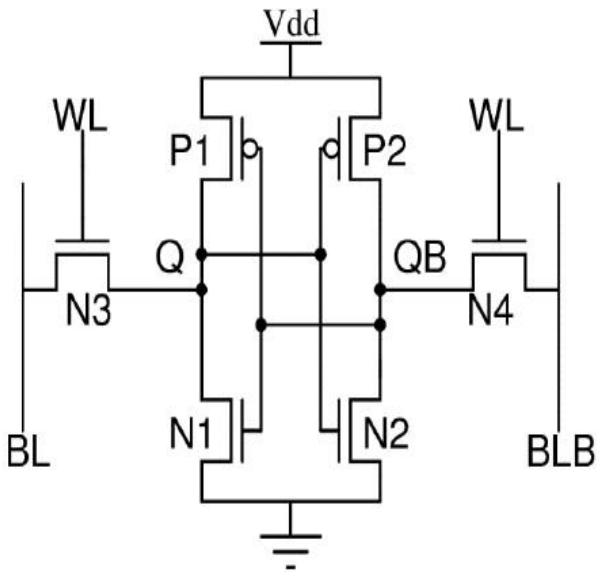


**Fig.2**Conventional 6T SRAM cell

## II. LITERATURE SURVEY

This part compares the overall performance of SRAM cells, including the different shapes of transistors that are kept a bit separate. For the last four decades, we will tend to reduce CMOS hardware to get the best overall performance in speed, power consumption, noise margins, shutdowns, etc., and top speed. However, due to the device's size, we tend to run into hard stops designed for SRAM's micromillimeter style. Due to the low threshold voltage and the ultra-thin gate compound, the excess energy withdrawal accelerated. Data balance is also affected during the browsing and writing process. Any other difficulties, such as random fluctuation of inclusions, line segment roughness, and compound thickness fluctuation, reduce the stability of mobile SRAM. During the analysis of the performance of this section of 6T, 8T has been implemented, and deferred power consumption has been.

**Soumitra et al. [2019]**Higher variable resilience, lower power consumption, and better reliability are the critical design metrics for SRAM cell design. The most intuitive way to achieve lower power consumption is to measure the voltage. However, scaling the voltage on the nanotechnology nodes ends up weakening the robustness of the mobile SRAM and lowering the register balance. The traditional SRAM 6T failed to hold its stability in the era of climbs, especially on the deep sub-threshold system. In addition,

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SRAM cells that use strategies such as read separation to achieve reliable studio operation tend to develop newer leaks that result in better energy retention, contributing to a large portion of the total power consumption. In modern network devices. It is proposed to use a fully SRAM based on the 9T gate drive, and it meets these requirements in exchange for a slightly higher write and test time to meet the requirements for better strength and lower standby power dissipation. Simulations are performed using a sixteen nm metal oxide semiconductor version.

**Tripathi et al. [2018]**The digital semiconductor industry is advancing at a breakneck pace. The life of mobile and portable devices is getting shorter by the day, and the demand for longer backup batteries is also increasing. With these requirements, standby power leakage becomes a significant problem for researchers. In most of these devices, memory is a vital part, and its size is also reduced as the length of the device is reduced. Therefore, the low-power and over-speed memory design are in a high position.Another important thing is the stability of the SRAM cells. This document combines fingertip and polynomial techniques to recommend a modified SRAM 6T cell that features the extra-fast, advanced balancing, and accidental leaks in the standby mode of memory cells. Simulations are performed using a Cadence Virtuoso on UMC 55 nm technology.

**Ahmad et al. [2018]**This paper provides a robust, low-dropout, fully 1/2-selection, 12-transistor-free (PD12T) SRAM cell with adequate static and dynamic erase/write performance. The proposed cell offers the best read/wait SNM, write margin (WM), and lowest leakage capacity among all the cells listed in this table while creating overhead space 2.5 times larger than the 6T cell. Simulation results at VDD = 0.5 V show that mobile PD12T provides 4.24 times better RSNM, 1.62 times more WM, and 1.9 times less leakage electricity (at 50°C) compared to 6T SRAM. The proposed cell presents a VDD, min = 140 mV, which is 260 mV smaller than the 6T cell. When operating at VDD, min, the proposed cell draws 13.6 times less than the average leakage power. The proposed mobile device has an Ion/Ioff ratio of more than 10× compared to a 6T cell and has the potential to catch up on top space by having a greater variety of cells connected to the same bit line.

**Vatajelu et al. [2011]**In this work, a measure is proposed to assess cell robustness in the presence of transient voltage indicators. Sufficiently high-power noise indicators will force the mobile

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phone to become a failed state. On the contrary, low enough electrical noise indicators will not be able to operate the mobile phone, and the country will be maintained. The dynamic noise margin measure (DNM) is the minimum energy of the voltage pulses capable of inverting the cell. A case example of transient pulses of voltage noise in a 6T SRAM cell was studied using a 45 nm epoch. Simulation results show the use of the proposed measure as a hallmark of force acting in the presence of short voltage noise.

**Lin et al. [2010]** This paper proposes a write-assisted asymmetric digital cellular ground bias, and feedback detection grandiose schemes to improve the study of static noise fringe (RSNM), write margin (WM), and transmission speed. Unparalleled 8 Mobile T SRAM read/write operation. The 4Kbit SRAM test chip is implemented in the 90nm CMOS generation. The validation chip size results show that at zero.2 Vd, an operating frequency of 6.0 MHz, can be completed with a power consumption of 10.4 µm.

**Shukla et al. [2019]**In this paper, a beefy SRAM was implemented based on the 13T-ST. Additionally, the overall performance of the SRAM 13T cell is compared to a conventional SRAM 6T cell. The comparator is made by changing the conduction voltage from 0.5V to 1V. In addition, we obtain access to the time, power, and static noise margin (SNM) for both designs. Simulation effects show that Schmidt reason-based 13T SRAM has 0.41x write '1' access time, 2.31x write SNM, 2.23x read SNM, 1.1x SNM in standby, 0.80x power leakage compared to conventional 6T SRAM at 700mV.

## III. PROPOSED 8T SRAM CELL

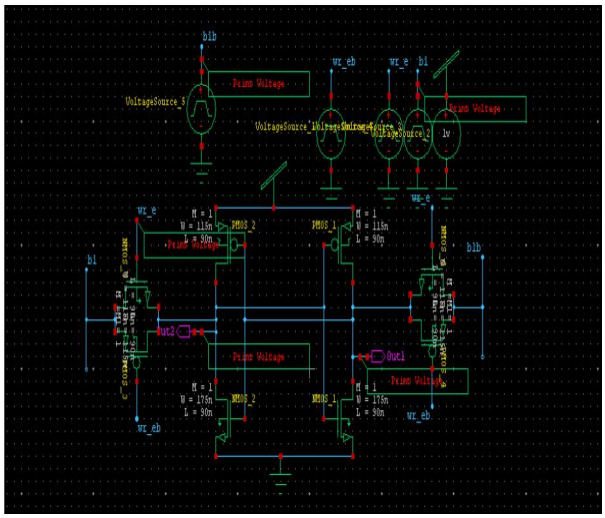

**Fig.3**Proposed 8T SRAM cell

Figure 3 shows the circuit diagram of the recently proposed SRAM 12T cell. The proposed design is identical to the previous 8TSRAM cell. Still, here we have made a modification that includes, instead, what we have achieved is that we have eliminated the voltage source used. So, the range of additives decreased. We have placed the TG at the NMOS location of each transistor short; This can guarantee 5real production ranges because we realize TG gain over MOS. And we can see the

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impact of those modifications on our results in the next section.

## DYNAMIC THRESHOLD MOS (DTCMOS)

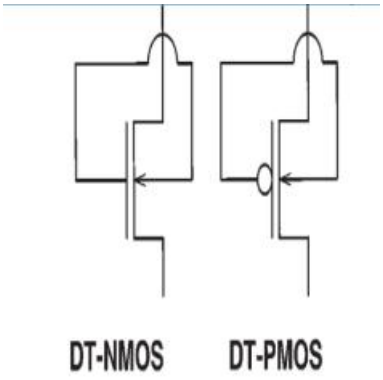


**Fig.4** Dynamic threshold NMOS and PMOS.

In a dynamic threshold MOS (DTMOS) topology, the gate of the transistor is connected to its substrate terminal, as shown in Fig. 4. Therefore, the substrate voltage is constantly changing with the gate voltage of the transistor. Trading in the substrate voltage dynamically changes the threshold voltage. DTMOS behaves just like a standard transistor in the world, ie. VIN = VDD (VIN = 0) for PMOS (NMOS). Both display the same parameters with departures from the current threshold

voltage. However, in the on state, as the gate-to-source (VGS) voltage increases, the substrate-to-source (VBS) voltage will also increase. This similarly lowers the edge voltage of the DTMOS transistor. The decrease in threshold voltage is due to lower frame costs which increase service mobility. This, in turn, reduces effective natural discipline. All these results combined lead to better modern operation on a DTMOS transistor, as shown in Figure IV.

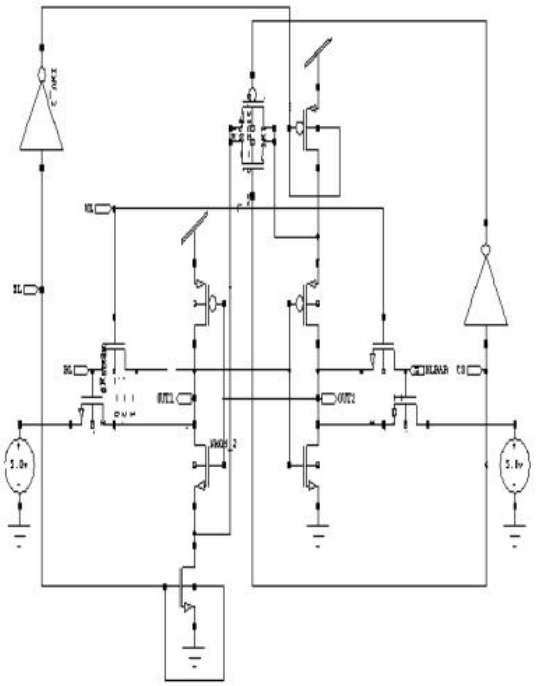

**Fig.5**SRAM DTCMOS

## IV. TRANSMISSION GATE

In principle, the transmit gate consists of field-effect transistors, where, unlike standard discrete field-effect transistors, the substrate (bulk) terminal is not internally connected to the source terminal. Transistors, n-channel MOSFETs, and p-channel MOSFETs are connected in parallel to this, but only the source and drain ends of the transistors are connected. Its gate terminals are connected through a

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NOT (inverter) gate to form a tamper terminal.

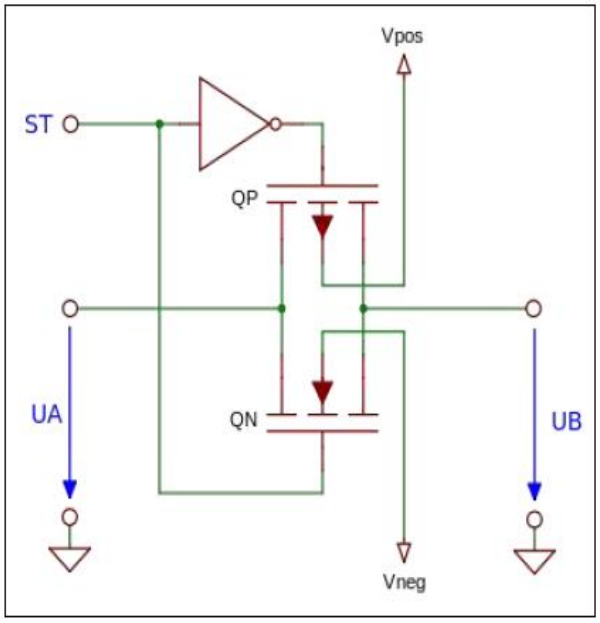


**Fig.6**Principal diagram of a transmission gate

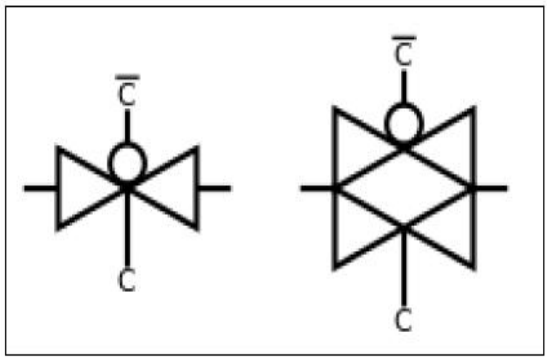


**Fig.7** Two variants of the "bow tie" symbol commonly used to represent a transmission gate

Two versions of the "bow-tie" symbol usually represent a transfer gate on circuit diagrams. Unlike discrete FET transistors, the substrate terminal is not connected to the supply connection. Instead, the substrate terminals are connected to a corresponding conduction voltage amplitude to ensure that the parasitic substrate diode (between gate and

substrate) is always reverse-biased and thus does not affect the waveform of the substrate. Signal. For this reason, the substrate terminal of the p-channel MOSFET is connected to a precise supply voltage capacity, and the substrate terminal of the n-channel MOSFET is connected to a weak supply voltage capacity.

A proposed design is simulated using Tanner EDA Tool using TSMC 90nm technology at 1V supply fig.6 shows outputwaveform of proposed 8TSRAM cell. Obtained result of new design is compared with old 8T SRAM cell and tabulated in table 1as shown.

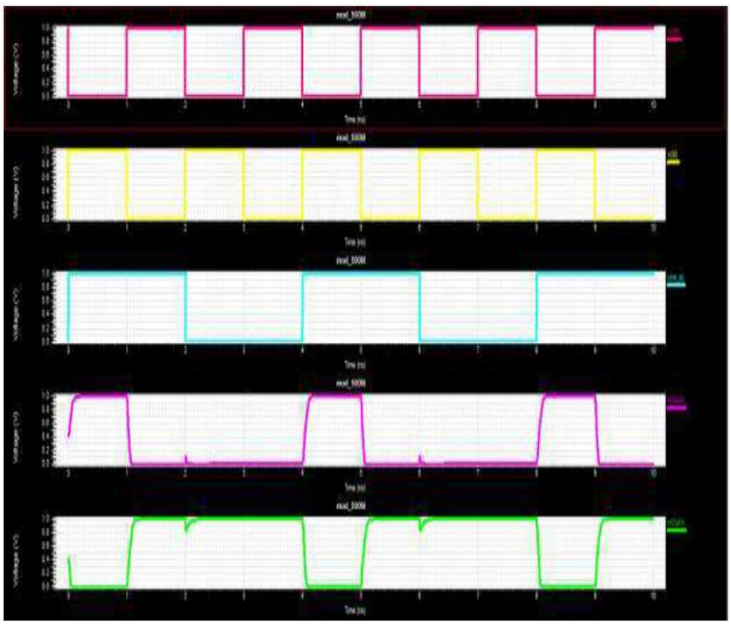

Fig.8Simulation Results of Proposed 8T SRAM Cell

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**Table.1**8T SRAM v/s Proposed 8T SRAM CELL Comparison

8T SRAM v/s Proposed 8T SRAM CELL Comparison

| Frequency (in HZ) | Power (in µW) | Write_1 | | Write_0 | |
|---|---|---|---|---|---|
| | | Delay (ps) | PDP (in a) | Delay (ps) | PDP (in a) |
| Base Designs | | | | | |
| 500M | 2.5731 | 74.940 | 192.828 | 45.319 | 116.610 |
| 1G | 4.8162 | 73.133 | 352.223 | 45.552 | 219.387 |
| 2G | 9.5662 | 73.084 | 699.136 | 45.542 | 435.663 |
| Modified Designs | | | | | |
| 500M | 0.6065 | 46.744 | 28.350 | 28.349 | 17.193 |
| 1G | 1.1601 | 47.548 | 55.160 | 27.739 | 32.180 |
| 2G | 6.7268 | 69.041 | 464.442 | 33.972 | 228.522 |

## V. CONCLUSION

Since generation changes every day, power dissipation and stability are the main difficulties of any high-speed device. The proposed SRAM cell is an answer to this problem that uses the transfer gate as the input gate of the transistor to generate less power dissipation with high-speed operation. The newly proposed SRAM 8T cell delivers high speed and much lower electricity than the previous design. The mentioned high-speed mobile SRAM can be used in a memory architecture consisting of flash memory. Simulations are performed using Tanner Tolls on TSMC 90nm technology.

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